Tektronix®
COMMITTED TO EXCELLENCE

PRISM 30MPM/30MPX MICROPROCESSOR MODULE

070-6673-00
Product Group 5E

First Printing: August 1989
Revised Printing: December 1989

Tektronix, Inc.
Walker Road Industrial Park
P.O. Box 4600
Beaverton, OR 97076

MANUAL REVISION STATUS

Product: 30MPM/MPX User's

REV DATE	DESCRIPTION
AUG 1989	First Printing
DEC 1989	Revised Pages-- i, ii, iii, iv, 2-1, 2-3, 2-4, 2-5, 2-8, 2-16, 2-22, 2-26 thru 2-29, 2-36 thru 2-39, 3-3, 3-9, 3-21, 3-22, 3-29, 4-2, 4-3, 4-4, 4-13, 4-30, 4-31, all of Section 5, all of Appendix B, all of the Glossary & Index.

Table of Contents

Section 1: PRODUCT DESCRIPTION

MANUAL CONVENTIONS 1-2
STATE SECTION 1-2
- Microprocessor Disassembly 1-3
- Prototype Debug Tool 1-3
- Performance Analysis 1-3

TIMING SECTION 1-4

Section 2: USING THE STATE SECTION

STATE SECTION DESCRIPTION 2-1
- P6480 Probe 2-2
- General Purpose Probe Adapter Leadset 2-3
- Other leadsets 2-5

GETTING STARTED WITH THE STATE SECTION 2-5
ACQUIRING DATA WITH THE STATE SECTION 2-5
- Setting Up the State Section 2-6
  - Acquisition Mode 2-8
  - Memory Depth 2-8
  - Number of Triggers 2-9
  - Trigger Location 2-9
- Defining the Acquisition Clock 2-11
  - Async 2-13
  - Sync 2-13
  - Demux 2-16
- Defining Channel Groups 2-19
  - Deleting Channels From Groups 2-22
  - Adding Channels To Groups 2-22
  - Joining Channel Groups 2-22
  - Splitting Channel Groups 2-23
- Defining the Trigger Specification 2-23
  - Defining Trigger Conditions 2-26
  - Defining a Test 2-33
  - Adding a Test 2-35
  - Adding a State 2-35
- Defining Actions 2-35
  - State Control Actions 2-36
  - General Actions 2-36
- Defining Global Storage Qualifications 2-38
- Making an Acquisition 2-40

DISPLAYING DATA WITH THE STATE SECTION 2-41

Section 3: USING THE TIMING SECTION

- P6486 Timing Probe 3-1
- Leadsets 3-2

GETTING STARTED USING THE TIMING SECTION 3-4

Example 1: Transitional Acquisition Mode 3-4
Example 2: Transitional Acquisition Mode Showing Bursts of Data 3-8
ACQUIRING TIMING DATA 3-12
Selecting the Acquisition Mode 3-16
Transitional Acquisition Mode 3-16
Synchronous Acquisition Mode 3-17
Timing Section Off 3-18
Selecting the Trigger Position 3-19
Selecting the Acquisition Threshold Voltage 3-20
Creating a Trigger Specification 3-21
Defining Channel Groups 3-21
Arming 3-25
Selecting a Trigger Test 3-26
Changing the Channel Group Radix 3-26
Choosing to Trigger on a True or False Event 3-27
Defining the Trigger Event Word Recognizer 3-27
Choosing the Action to Perform 3-27
DISPLAYING TIMING DATA 3-28
Acquisition Status Screen 3-28
Timestamp Values and Shared Memory 3-28
SAVING TIMING SECTION SETUPS 3-30
SAVING TIMING SECTION DATA 3-30

Section 4: USING MNEMONIC DISASSEMBLY
How to Use This Section 4-1
Disassembler Components 4-1
GETTING STARTED WITH MNEMONIC DISASSEMBLY 4-2
INSTALLING THE DISASSEMBLER 4-2
Installing the Software in the Mainframe 4-2
Hard Disk Installation 4-2
Floppy Disk Installation 4-3
Making Connections 4-3
Connecting the P6480 Probe to the Mainframe 4-4
Connecting the Disassembler Probe Adapter to the P6480 4-5
Connecting the Disassembler Probe Adapter to the SUT 4-6
Loading the Software 4-16
ACQUIRING DATA WITH A DISASSEMBLER 4-17
Selecting the Clocking Mode 4-18
Viewing the Channel Groupings 4-20
Defining Symbols 4-21
Defining the Trigger 4-23
Making the Acquisition 4-23
VIEWING DATA WITH A DISASSEMBLER 4-23
State Table 4-24
Hardware 4-25

Software 4-26
Control Flow 4-27
Subroutine 4-28
DISPLAY FEATURES 4-29
Special Characters 4-29
Processor Support 4-29
Mark Cycle 4-30
Split Screen Display 4-31

Section 5: USING THE PROTOTYPE DEBUG
PDT THEORY OF OPERATION 5-2
STEPS TO USE THE PDT 5-4
1. Install the PDT Software 5-4
2. Set Up the PDT Configuration Submenu 5-4
3. Make Hardware Connections 5-4
4. Load Program into PDT 5-4
5. Debug Your Program 5-4
ADVANTAGES OF USING PDT 5-5
APPLICATIONS FOR PDT 5-5

Appendix A: INSTALLING SOFTWARE
Hard Drive A-1
Floppy Drive A-1
INSTALLING HARDWARE A-1

Appendix B: SPECIFICATIONS
CHARACTERISTICS/SPECIFICATIONS B-1

Appendix C: OPTIONS AND ACCESSORIES
MPM/MPX OPTIONAL ACCESSORIES C-1
DISK MNEMONICS PRODUCTS C-1
30DM04 8086/8088 Mnemonic Disassembly C-1
Standard Accessories C-1
Optional Accessories C-1
30DM06 80186/80188 Mnemonic Disassembly C-2
Standard Accessories C-2
Optional Accessories C-2
30DM08 80286 Mnemonic Disassembly C-2
Standard Accessories C-2
Optional Accessories C-2
30DM09 80386 Mnemonic Disassembly C-2
Standard Accessories C-2
Optional Accessories C-3
30DM27 68000/10 Mnemonic Disassembly C-3
Standard Accessories C-3
Optional Accessories C-3
30DM31 68020 Mnemonic Disassembly C-3
Standard Accessories C-3

Optional Accessories C-3
30DM33 68030 Mnemonic Disassembly C-4
Standard Accessories C-4
Optional Accessories C-4
30DM41 Z80 Mnemonic Disassembly C-4
Standard Accessories C-4
Optional Accessories C-4
PERFORMANCE ANALYSIS C-4
PROTOTYPE DEBUG TOOL PRODUCTS C-4
30RP1 General Purpose Prototype Debug Tool with ROM Probe C-4
Standard Accessories C-4
Optional Accessories C-5
30DD27 68000/010 Prototype Debug Tool C-5
Standard Accessories C-5
30RP1 General Purpose Prototype Debug Tool with ROM Probe C-5
Optional Accessories C-5
FasTrak Products C-5
FasTrak Microprocessor Training Package Standard Accessories C-5
FasTrak Microprocessor Training Package Optional Accessories C-5

GLOSSARY

INDEX

List of Figures

Figure 2-1. P6480 connected to the mainframe. 2-2
Figure 2-2. GPPA connected to the P6480. 2-4
Figure 2-3. State Section Setup menu. 2-7
Figure 2-4. Memory Depth. 2-9
Figure 2-5. Trigger Location. 2-10
Figure 2-6. Clocking/Grouping submenu. 2-12
Figure 2-7. Synchronous Clocking submenu. 2-14
Figure 2-8. Demux Clocking submenu. 2-17
Figure 2-10. Channel Grouping submenu. 2-20
Figure 2-12. State Section Setup menu showing conditions, tests, and states. 2-25
Figure 2-13. Define Conditions submenu. 2-27
Figure 2-14. Word Recognizer Condition. 2-28
Figure 2-15. Counter Condition. 2-30
Figure 2-16. Timer Condition. 2-31
Figure 2-17. Signal Condition. 2-32
Figure 2-18. Test Components. 2-33
Figure 2-19. Global Storage Qualification fields. 2-39
Figure 3-1. Connecting the P6486 Timing probe. 3-3
Figure 3-2. FasTrak circuit board pin locations. 3-5
Figure 3-3. Plain transitional acquisition data. 3-7
Figure 3-4. Magnified plain transitional acquisition data. 3-8
Figure 3-5. Data bursts captured using transitional acquisition mode. 3-10
Figure 3-6. Magnified data burst using split screen. 3-11
Figure 3-7. Fully-magnified data burst. 3-12
Figure 3-8. Timing Section setup menu. 3-14
Figure 3-9. Transitional acquisition storage versus traditional asynchronous storage. 3-17
Figure 3-10. Minimum setup and hold times for synchronous mode using the standard leadset. 3-18
Figure 3-11. Trigger location. 3-19
Figure 3-12. Channel Grouping submenu showing the default setup. 3-23
Figure 3-13. Data rate versus number of data samples stored in memory. 3-29
Figure 4-1. P6480 probe connected to the mainframe. 4-4
Figure 4-2. Disassembly probe adapter connected to P6480. 4-6
Figure 4-3. Connecting the disassembly probe adapter to a socketed DIP. 4-7
Figure 4-4. Connecting the disassembly probe adapter to a soldered DIP. 4-9
Figure 4-5. Connecting the disassembly probe adapter to a socketed PGA. 4-11
Figure 4-6. Connecting the disassembly probe adapter to a socketed PLCC. 4-13
Figure 4-7. Connecting the disassembly probe adapter to a soldered PLCC. 4-15
Figure 4-8. State Section Setup menu. 4-18
Figure 4-9. Clocking Definition submenu. 4-19
Figure 4-10. Channel Grouping submenu. 4-20
Figure 4-11. Symbol Definition Menu. 4-22
Figure 4-12. State Table Display. 4-24
Figure 4-13. Hardware Display. 4-25
Figure 4-14. Software Display. 4-26

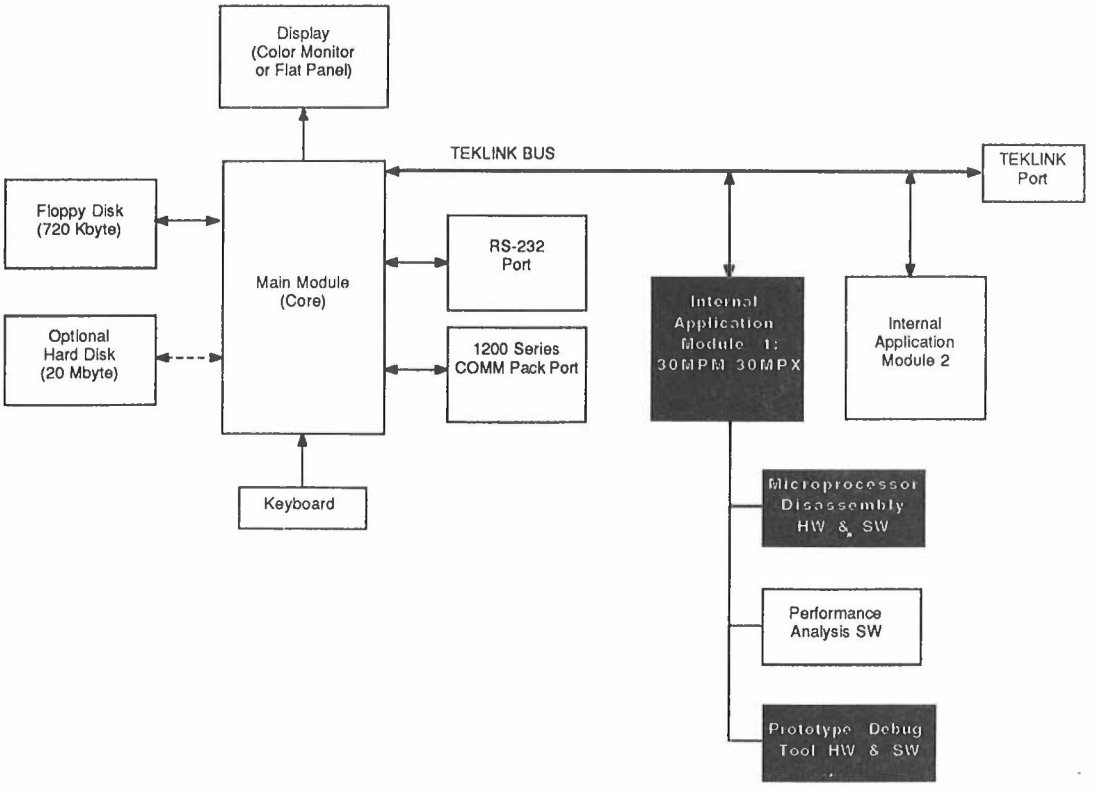
Figure 4-15. Control Flow Display. 4-27
Figure 4-16. Subroutine Display 4-28
Figure 4-17. Processor Support Submenu. 4-30
Figure 5-1. A PDT configuration. 5-3

List of Tables

Table 2-1. Asynchronous Clocking Speeds 2-13
Table 2-2. Clock Definitions 2-15
Table 2-3. Qualifier Definitions 2-15
Table 2-4. Illegal Clock and Qualifier Combinations 2-15
Table 2-5. Channel Groupings 2-21
Table 2-6. Word Recognizer Condition Test Symbols 2-29
Table 2-7. Counter Condition Test Symbols 2-31
Table 2-8. Timer Condition Test Symbols 2-32
Table 3-1. Standard Leadset Color Channel Number 3-3
Table 3-2. MPM Connections for Example 1 3-5
Table 3-3. MPM Connections for Example 2 3-9
Table 3-4. Acquisition Threshold Voltages 3-21
Table 3-5. Acquisition Window Size 3-30
Table B-1. 30MPM/MPX Functional Requirements B-2
Table B-2. 30MPM/MPX Performance Requirements B-6
Table B-3. 30MPM/MPX Environmental Specifications B-8
Table B-4. 30MPM/MPX Physical Specifications B-8
Table B-5. 30MPM/MPX Safety and Regulatory Specifications B-9
Table B-6. 30MPM/MPX Reliability Specifications B-9
Table B-7. P6480 State Probe Functional Requirements B-10
Table B-8. P6480 State Probe Performance Requirements B-11
Table B-9. P6480 Probe Environmental Specifications B-12
Table B-10. P6480 Probe Physical Specifications B-12
Table B-11. P6480 Probe Safety and Regulatory Specfications B-13
Table B-12. P6480 Probe Reliability Specifications B-13
Table B-13. GPPA Leadset Performance Requirements B-14
Table B-14. GPPA Leadset Physical Specifications B-14
Table B-15. GPPA Leadset Reliability Specifications B-14
Table B-16. P6486 High-Speed Probe Functional Requirements B-15
Table B-17. P6486 High--Speed Probe Performance Requirements B-15
Table B-18. P6486 High-Speed Probe Environmental Specifications B-18
Table B-19. P6486 High-Speed Probe Physical Specifications B-18
Table B-20. P6486 High-Speed Probe Safety and Regulatory Specifications B-19
Table B-21. P6486 High-Speed Probe Reliability Specifications B-19
Table B-22. Standard Leadset Physical Specifications B-20
Table B-23. Standard Leadset Reliability Specifications B-20
Table B-24. High-Performance Leadset Physical Specifications B-20
Table B-25. P6480 Pin-To-MPM/MPX Channel B-21

Preface: A GUIDE TO PRISM 3000 DOCUMENTATION

PRISM 3000 series documentation consists of a number of different manuals. These manuals provide you with all the information necessary to install, operate, maintain, and service any PRISM 3000 mainframe and associated application modules. The following figure provides an overview of the PRISM system. The shaded areas in the figure represent the parts of the system that are discussed in this manual.



Overview of Prism 3000 System

The PRISM 3000 documentation consists of the following types of manuals:

- This 30MPM/30MPX Application Module User's Manual provides information on using the 30MPM/30MPX Application Module and the various microprocessor support options available for use with it. For more detailed information about

the contents of this manual, see How to Use this Manual near the end of this preface.

- A **system user's manual** for each type of PRISM 3000 mainframe (3002 or 3001). These manuals include a basic introduction to operating the PRISM 3000 mainframe, a discussion of PRISM 3000 system-level menus, and reference information such as external device connection procedures, specifications, and a glossary of terms.
- A quick **reference guide** that briefly describes each PRISM 3000 menu.
- An on-line documentation package that consists of **Notes** that you can call up on the display screen to explain specific menu functions.
- A series of **application module user's manuals** that explain how to use each of the PRISM 3000 application modules.
- A series of **application software user's manuals** that describe the various application software packages.
- A series of **microprocessor-specific mnemonic disassembly user's manuals** (designed to be used with the *30MPM/MPX Application Module User's Manual*). These options allow you to disassemble microprocessor signals into their assembly-language equivalents.
- A series of **microprocessor-specific prototype debug tool user's manuals** (designed to be used with the *30MPM/MPX Application Module's User's Manual*) that describe how to use the debug tools to troubleshoot your microprocessor-based prototypes.
- A series of **service manuals** that help qualified technicians maintain, troubleshoot, and repair PRISM 3000 series mainframes and application modules. These manuals also contain procedures for performing incoming inspections, verifying performance specifications, and making system adjustments.

Appendix C: Options and Accessories contains a list of available PRISM 3000 manual titles and Tektronix part numbers.

HOW TO USE THIS MANUAL

If your PRISM 3000 hardware has not been set up, read and follow the installation procedures in Appendix A of your system user's manual.

The *PRISM 3002 System User's Manual* is the master reference document for the entire PRISM 3000 system. (If you are using a system built around a PRISM 3001 mainframe, use the *PRISM 3001 System User's Manual* as the master reference document.) If you are unfamiliar with the PRISM 3000, use this manual to learn how to use the mainframe and the system-level menus. If you are an experienced PRISM 3000 user, use this manual as a reference document to look up specific functions and to acquaint yourself with the various configurations, options, and accessories available for the system. This manual comprises the following sections:

- **Section 1: 30MPM/30MPX Application Module Description**. Contains an overview of the 30MPM/30MPX Application Module along with descriptions of the microprocessor support options available for use with it.
- **Section 2: Using the State Section**. Contains details of the features of the State Section, including how to use multi-level triggering.
- **Section 3: Using the Timing Section**. Contains details of the features of the Timing Section, including how to make transitional or synchronous acquisitions.
- **Section 4: Using Mnemonic Disassembly**. Contains general information about Mnemonic Disassembly, including how to make hardware connections to the SUT, how to set up to make an acquisition, and describes features of the mnemonic disassembly display.
- **Section 5: Using the Prototype Debug Tool**. Contains general information about the Prototype Debug Tool.
- **Appendix A: Installing Software**. Contains information about installing software that comes with the 30MPM/30MPX Application Module.
- **Appendix B: Specifications**. Contains electrical, mechanical, and environmental specifications for 30MPM/30MPX Application Module.
- **Appendix C: Options and Accessories**. Lists the available 30MPM/30MPX Application Module options and accessories (both standard and optional).
- **Glossary**. Defines terms specific to the 30MPM/30MPX Application Module and terms that pertain to logic analysis in general.
- **Index**. At the back of this manual, you will find an index to help you locate information on specific subjects in this manual.

GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply, and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as you read the marking, or a hazard to property including the equipment itself.

WARNING indicates only a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting it to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The main disconnection is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power-up the instrument until such objects have been removed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury or damage to the product, do not operate this product with covers or panels removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not return the instrument to service until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: PRODUCT DESCRIPTION

The 30MPM/30MPX application module can be used in any of the PRISM 3000 Series mainframes. The 30MPM/30MPX module has all the instruments you need on a single module for microprocessor analysis to solve the full range of design needs for microprocessor-based systems. This application module performs as a state and microprocessor analyzer, a timing analyzer, a microprocessor disassembler and performance analyzer, and a firmware debugger.

The 30MPM/30MPX application module is suitable for applications involving:

- software verification
- software debugging
- software optimization
- hardware/software integration
- microprocessor integration
- multi-processor integration

The 30MPM and the 30MPX application modules are similar to each other, differing only in the number of acquisition channels each module provides: the 30MPM provides 64 state acquisition channels and can support 8- and 16-bit microprocessors. The 30MPX provides 96 state acquisition channels and can support 8-, 16- and 32-bit microprocessors.

The 30MPM/30MPX module supports microprocessors with clock rates of up to 33 MHz. It can store up to 8 kilobytes of acquisition data. It also provides nine 200 MHz timing acquisition channels.

The 30MPM/30MPX application module consists of two sections: the State Section and the Timing Section. Data can be acquired with either section and viewed in a variety of formats. The State Section acquires data from 8-, 16-, and 32-bit microprocessors. The State Section also provides the basis for microprocessor disassembly and firmware debugging capabilities. The Timing Section provides high resolution timing information on a smaller number of channels.

Module. An individual functioning acquisition unit of a PRISM mainframe.

Section. One part of a module, i.e., the State Section or the Timing Section.

Each section is capable of sending and receiving signals. Signals can be sent to another section of the same module, to another module, or to another device.

MANUAL CONVENTIONS

This manual uses the following conventions:

- SUT refers to the system under test.
- An X represents Don't Care when designating binary signal values.
- PRISM refers to any of the PRISM 3000 Series mainframes.
- Unless otherwise noted, MPM refers to either the 30MPM or 30MPX application module.

STATE SECTION

The State Section of the MPM module samples and stores digital data taken from a system under test. The data stored can then be viewed in different formats for analysis. It is useful for analyzing hardware and software systems and for resolving digital circuitry problems.

The State Section is capable of acquiring data from 8-, 16-, and 32-bit microprocessors. Up to 8 kilobytes of bus cycles can be stored. Stored data is time-stamped so it can be correlated with data from the Timing Section of the MPM or from other modules in the PRISM system. The timestamping resolution is 20 ns.

The trigger specification can consist of up to seven states (or levels). Each state can have up to eight tests with related actions. Each test can include up to 4 of a possible 20 conditions, consisting of word or range recognizers, counters, timers, and intermodule signals. Trigger specification components work together to form a complex multi-state trigger machine with a variety of actions attached to each state.

For more information on the State Section, refer to section *Using the State Section* in this manual.

Microprocessor Disassembly

The MPM module supports mnemonic disassembly and analysis for a variety of popular microprocessors. This support consists of a probe adapter (which has been configured for the particular microprocessor you are disassembling), software to disassemble the signals from the microprocessor, and a manual with information that is specific to the microprocessor your disassembler supports.

For more information on microprocessor disassembly refer to the section *Using Mnemonic Disassembly* in this manual.

Prototype Debug Tool

The Prototype Debug Tool (PDT) is a new approach to developing processor-based prototype systems. PDT consists of hardware and software that provide an interface to the memory of a prototype or other system under test. PDT is the tool of choice in the early phases of developing a new system that incorporates an embedded microprocessor. It helps you develop, troubleshoot and debug microprocessor hardware and system firmware and software.

When properly interconnected between an MPM or MPX module and your prototype, PDT lets you run and control your hardware from the keyboard and screen of your PRISM 3000. With PDT you can download programs, view SUT register contents, patch SUT memory, set breakpoints, and single-step through code.

For more information on PDT, refer to the section *Using the Prototype Debug Tool* in this manual.

Performance Analysis

The PRISM Performance Analysis (PA) software is a versatile tool for evaluating the software performance of microprocessor-based systems. PA gives you real-time analysis to show you where programs are spending the most time.

Performance analysis software processes raw data acquired from the control, address, and data lines of a microprocessor-based system into a form that provides meaningful information about the system's performance characteristics. Based on PA's display, you can determine such things as overall system activity, the number of times a routine executes, and the amount of time the system spends in various defined regions.

For more information on Performance Analysis, refer to the *DA01 Performance Analysis Application User's Manual.*

TIMING SECTION

The Timing Section of the MPM application module functions independently of the State Section. Use the Timing Section to look at timing on the control bus. The Timing Section samples data, searches for a trigger event, stores data, and performs an action. Nine channels can be used to define one trigger event word. You can acquire data samples at a maximum rate of one sample every 5 ns (200 MHz).

For more information on the Timing Section, refer to section *Using the Timing Section* in this manual.

Section 2: Using the State Section

This section contains information on how to use the State Section of the MPM module, including information about probes, leadsets, triggering specifications and data display.

STATE SECTION DESCRIPTION

The State Section of the MPM module is a logic state analyzer. It samples and stores digital data taken from a system under test. The data stored can then be viewed in different formats for analysis. It is useful for analyzing hardware and software systems and for resolving digital circuitry problems.

The State Section is capable of acquiring data on 64 or 96 channels. Up to eight kilobytes of samples can be stored. Data stored is time-stamped so it can be correlated with data from the Timing Section of the MPM or from other modules in the PRISM mainframe. Timestamping resolution is 20 ns.

The trigger specification can involve seven states. Each state can have up to eight tests with related actions. Each test can include up to four of a possible 20 conditions, consisting of word or range recognizers, counters, timers, and intermodule signals. Trigger specification components work together to form a complex multi-state trigger machine with a variety of actions attached to each state.

In order to use the State Section, you must make three connections. Be sure the power to the SUT is off before performing the following steps:

1. Connect the P6480 state probe to the mainframe.
2. Connect a leadset to the P6480 probe.
3. Connect the leadset to the SUT.

CAUTION

To avoid damage to the SUT, be sure the power to it is off before making any probe or leadset connections. To avoid damage to the PRISM, power down the SUT before powering down the PRISM.

Descriptions of the probe and leadsets and their installation instructions follow.

P6480 Probe

The P6480 State Probe is used to make an acquisition with the State Section.

Probe. The hardware which connects the mainframe to a leadset, usually composed of a connector to the mainframe, a cable, a plastic housing containing a circuit board, and a connector to the leadset.

Leadset. The hardware which connects the probe to the SUT, usually composed of a connector to the probe, a plastic housing which sometimes contains a circuit board, and cables or leads with connectors which attach to the SUT.

To connect the P6480 State Probe to the mainframe, insert the P6480 State Probe cable connector into the State Section slot on the mainframe. The State Section slot is the one closest to the rear of the mainframe. This slot is keyed so that only the State Probe cable connector will fit in it and the State Probe cable connector will only fit one way.

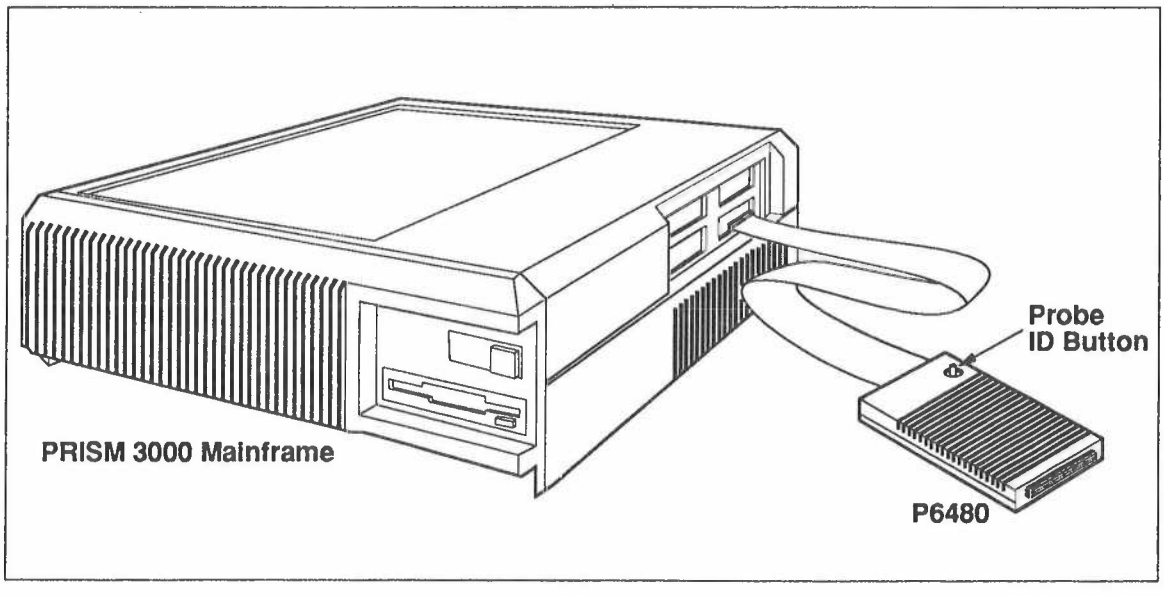


Figure 2-1. P6480 connected to the mainframe.

Press the button labeled ID on the probe for probe and leadset information.

To identify which State Section the state probe is connected to, press the button labeled "ID" on the P6480. The module and section number to which the state probe is connected will be displayed on the top line of the screen. An example of such an ID number is "MPM1: Internal Probe 1 with No Leadset."

General Purpose Probe Adapter

The General Purpose Probe Adapter (GPPA) is a 96-channel leadset. If you have an MPM application module, you can only use channels 0 through 63. If you have an MPX application module, you can use channels 0 through 95.

One end of the GPPA has a plastic housing with a connector to connect to the P6480 State Probe. The GPPA has two wide cables and one narrow flat cable at one end. The two wide flat cables divide into 88 separate leads, each tipped with a barrel connector. The barrel connectors may be used directly on pins on the SUT or may be used with grabber tips (Tektronix part number 020-1386-01, package of 12).

The narrow flat cable is divided into eight twisted pairs. Each channel has its own ground. One lead in each pair is labeled with a channel number 0 through 7; the other lead in each pair is the ground and is labeled "GND." These are used to acquire channels 0 through 7. These lines are also used as clock and qualifier lines. Figure 2-2 shows the GPPA connected to the P6480. For clarity, Figure 2-2 shows only some of the leads.

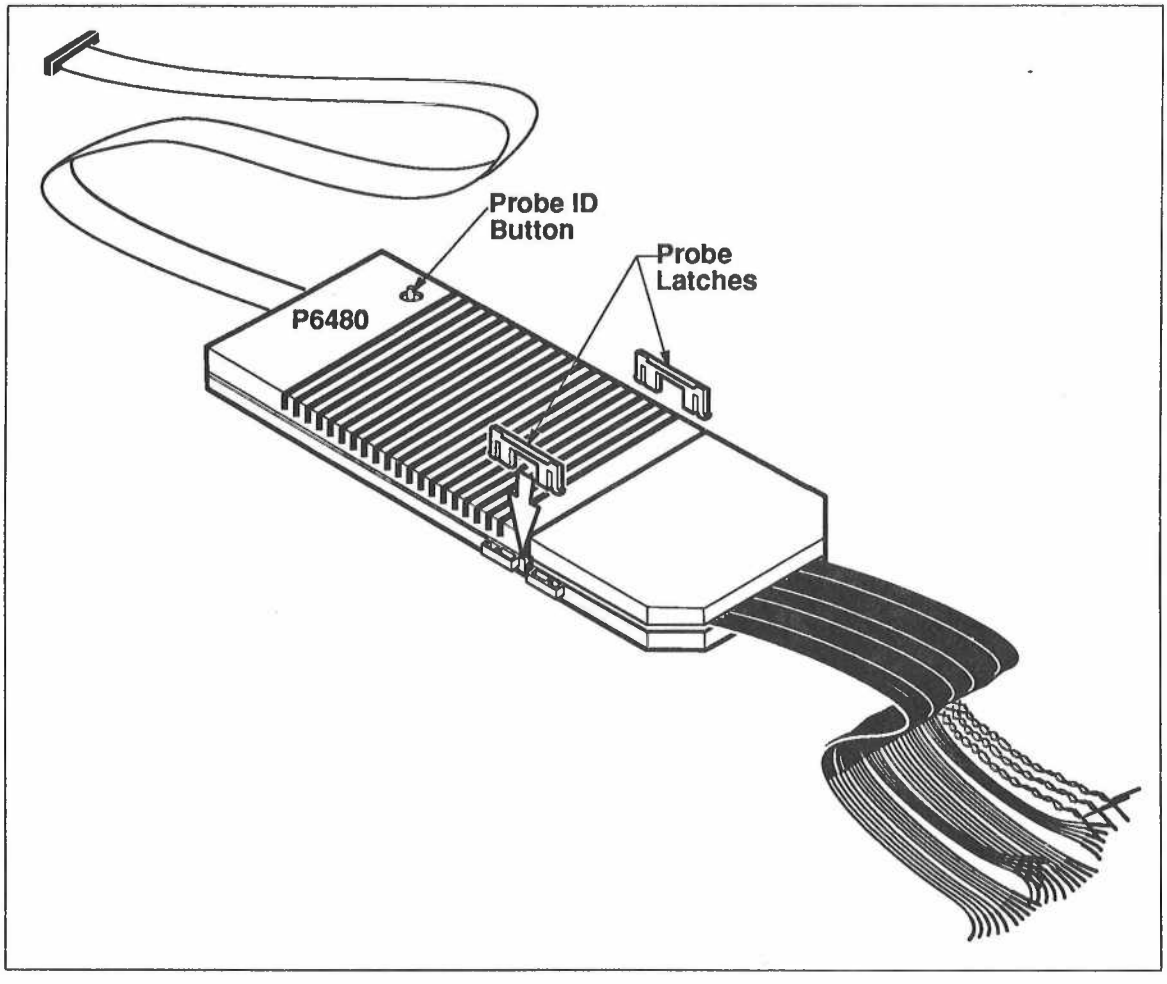


Figure 2-2. GPPA connected to the P6480.

The two wide flat cables are divided into 11 groups. Each group contains eight channels and two grounds. Each group is labeled with the range of channels contained in the group. The groups which can only be used with an MPX board are labeled MPX. Each channel lead is labled with its channel number and each ground is labeled "GND." MPM or MPX leads have blue lead tips, ground leads have black lead tips, and MPX-only leads have white lead tips.

NOTE

Read "Defining Channel Groups" later in this section for information on probing considerations before probing your system.

To connect the GPPA leadset to the P6480 State Probe perform the following steps:

1. Align the connector of the GPPA (label side up) with the connector of the P6480 (label side up).
2. Plug the GPPA into the P6480. The connectors on both the GPPA and the P6480 are keyed, so you cannot plug them in wrong.
3. Insert the probe latches by pushing the points of the latches into the loops of the probe and leadset.

Other leadsets

Special purpose leadsets other than the GPPA are available for use with the State Section. These include disassembler leadsets. When you purchase a disassembler, you will receive a special leadset to use with it. For information about these leadsets, refer to the section *Using Mnemonic Disassembly* in this manual.

GETTING STARTED WITH THE STATE SECTION

Using the FasTrak board, you can quickly take a data acquisition that will show you the State Table display. Perform the following steps:

1. Make sure the PRISM and the FasTrak are powered off.
2. Plug the P6480 into the mainframe.
3. Plug the P6480 into the connector labeled J100 on the FasTrak. Note that no leadset is necessary.
4. Power up the PRISM.
5. Power up the FasTrak.
6. Press and hold the reset button on the FasTrak while you press Start/Stop on the PRISM.
7. Release the reset button on the FasTrak.
8. When the acquisition is complete, the State Table will be displayed.

ACQUIRING DATA WITH THE STATE SECTION

To make a data acquisition, you must set up the acquisition clock, channel groups, trigger conditions, trigger specifications, and any storage qualifications.

Acquisition. The sampling of data from a system under test by a logic analyzer.

Acquisition Clock. The clock that determines the point in time at which the logic analyzer samples data.

Channel Groups. A defined organization of a number of inputs to form a meaningful combination, such as a 16-bit or 32-bit word.

Trigger. A test which, when met, causes the analyzer to initiate one or more actions.

This section will step you through setting up these parameters and will explain the options available for each parameter.

Setting Up the State Section

Press the Setup key. The cursor will be on the first field at the top line of the screen. This field allows you to choose the MPM module. This field also allows you to choose between the State Section and the Timing Section of the MPM module. With the cursor on the menu select field, press SELECT to cycle through the choices to select the correct slot and the State Section.

For information on loading an application, refer to the section *Using Utilities* in your system user's manual.

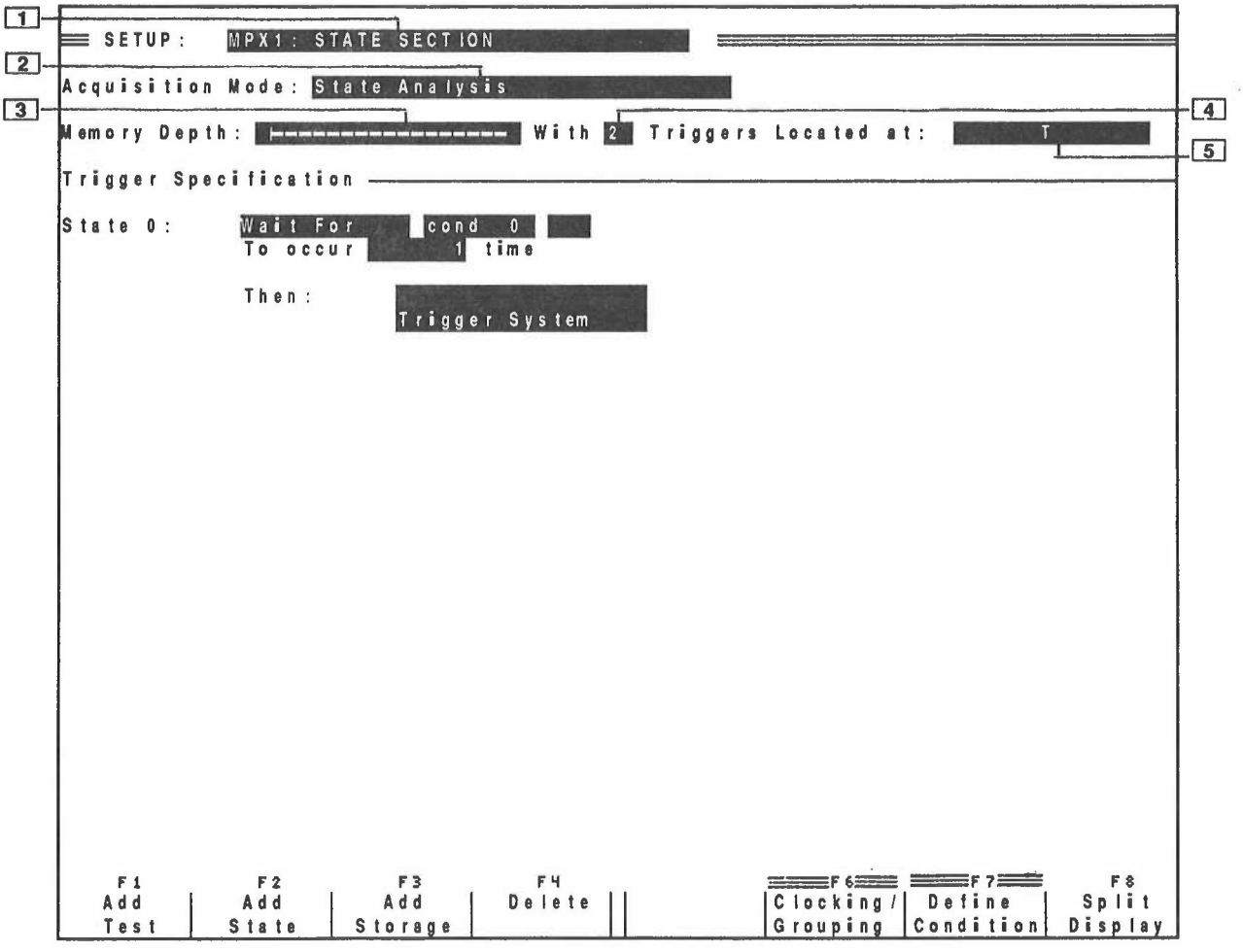


Figure 2-3. State Section Setup menu.

1 **Menu Select.** Allows you to select the MPM module and State or Timing Section.

2 **Acquisition Mode.** Allows you to choose State Analysis or Off. Allows you to select a disassembler, if disassemblers are loaded.

3 **Memory Depth.** Allows you to choose one of five memory depths.

4 **Number of Triggers.** Allows you to choose the number of triggers. Multiple triggers are available only if full memory depth is selected.

5 **Trigger location.** Allows you to choose where the trigger lies in relation to the whole memory partition.

Function keys

F6: Clocking/Grouping. Allows you to access the Clocking or Channel Grouping submenus.

Acquisition Mode

Make sure the Acquisition Mode field is set to State Analysis. You can turn off the State Section by cycling through this field to Off.

If you see something other than State Analysis or Off in the Acquisition Mode field, this indicates that disassembly software has been loaded automatically because a disassembly leadset is connected to the state probe. If you don't want to use the disassembler features, you can remove the disassembly leadset and power up the system again or you can unload the application.

For instructions on how to unload an application, see the section *Using Utilities* in the PRISM system user's manual.

Memory Depth

Choose your memory depth by cycling through the five memory depth choices. Each choice indicates the amount of total memory that will be used to store the acquisition. Total memory available to store acquisitions in an MPM module is 8 kilobytes of samples.

Memory Depth. The amount of memory set aside to store a acquisitions.

Memory Partition. The proportion of memory set aside for each trigger when using more than one trigger. When more than one trigger is specified, the partition for each trigger will be the same size.

If you have more than one grigger, the memory is partitioned. Figure 2-4 shows the memory depth selections and the proportional amount of the total memory depth represented.

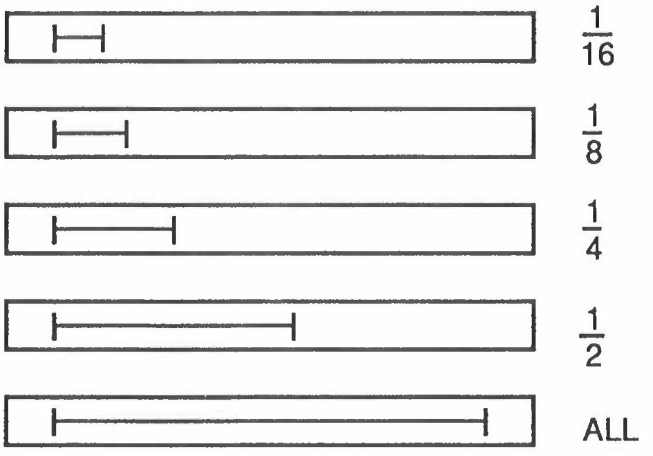


Figure 2-4. Memory Depth.

Number of Triggers

You can only use more than one trigger if you choose maximum memory depth.

You can use more than one trigger if you choose the maximum memory depth. After selecting the maximum memory depth, the number of triggers field appears. You can change the number of triggers by moving the cursor to the number of triggers field and pressing SELECT to cycle through the choices. You may have 1, 2, 4, 8, or 16 triggers defined.

When you define more than one trigger you are dividing the memory into that many equally sized partitions. All the partitions use the same trigger specification. When you press Start/Stop to make an acquisition, the first partition will begin to fill. When the trigger is encountered, the analyzer will finish filling the first partition with the specified amount of post-fill data. Then the trigger will reset and the analyzer will begin to fill the second partition. When the trigger condition is encountered again, the analyzer will finish filling the second partition with the specified amount of postfill data and reset the trigger. This continues until the specified number of triggers have caused each partition to fill. The data from each partition will be in the acquisition memory. In the data display, the first trigger (the oldest trigger) will be in the trigger location.

Trigger Location

The trigger location determines the amount of pre- and post-trigger memory that is filled (called pre-fill and post-fill).

Pre-fill memory. That part of the acquisition stored before the trigger event.

Post-fill memory. That part of the acquisition stored after the trigger event.

Choose the trigger location by placing the cursor on the Trigger Location field and pressing SELECT to cycle through the five trigger location choices.

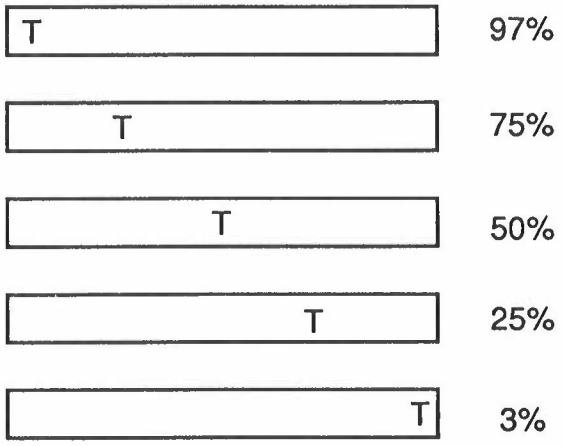


Figure 2-5. Trigger Location.

Figure 2-5 shows the visual representation on the screen and the amount of post-fill memory (as a percentage of total memory) represented by each trigger location choice. The rectangle represents the total memory available in the system. The T represents the location of the trigger in relation to the total memory.

Some examples of where to position the trigger are as follows:

- Position the trigger near the beginning of memory if you want to view the data samples occurring after the trigger event.
- Position the trigger near the end of memory if you want to view the data samples occurring prior to the trigger event.
- Position the trigger in the middle of memory if want to view the data samples occurring both before and after the trigger event.

NOTE

If the trigger condition is met on the first sample acquired, the trigger will be displayed at the first location, regardless of which trigger location was selected because there will be no pre-fill data.

The acquisition does not end until post-fill is complete. If your trigger specification is such that the post-fill is never completed, the acquisition never ends. Press the Start/Stop key to recover.

Defining the Acquisition Clock

The acquisition clock definition determines the sample points at which data is acquired.

Asynchronous Clocking. Clocking that is not related to the SUT's clock.

Synchronous Clocking. Clocking that is tied to the SUT's clock.

Multiplexed Clocking. A two-phase clock, allowing samples to be taken at either of two points in time.

There are three clocking modes: asynchronous, synchronous, and demultiplexing.

- Asynchronous mode. Sample points are determined by the analyzer at a speed you choose.
- Synchronous mode. Sample points occur with the SUT's clock.
- Demultiplexing mode. A two-phase sample is taken. You can set up two synchronous clocks to perform two-state clocking to allow you to acquire data from multiplexed lines, or from separate lines with alternating clocks.

While in the State Section Setup menu, press F6: Clocking/ Grouping to access the clock definition submenu. See Figure 2-6 to see the Clocking/Grouping submenu. This submenu is used to define clocking and channel grouping. The first field in this submenu toggles between Group Definition and Clock Definition. Press the SELECT keys to cycle to Clock Definition. The next field is Clock Type. Press the SELECT keys to cycle through the three choices: Async, Sync, or Demux.

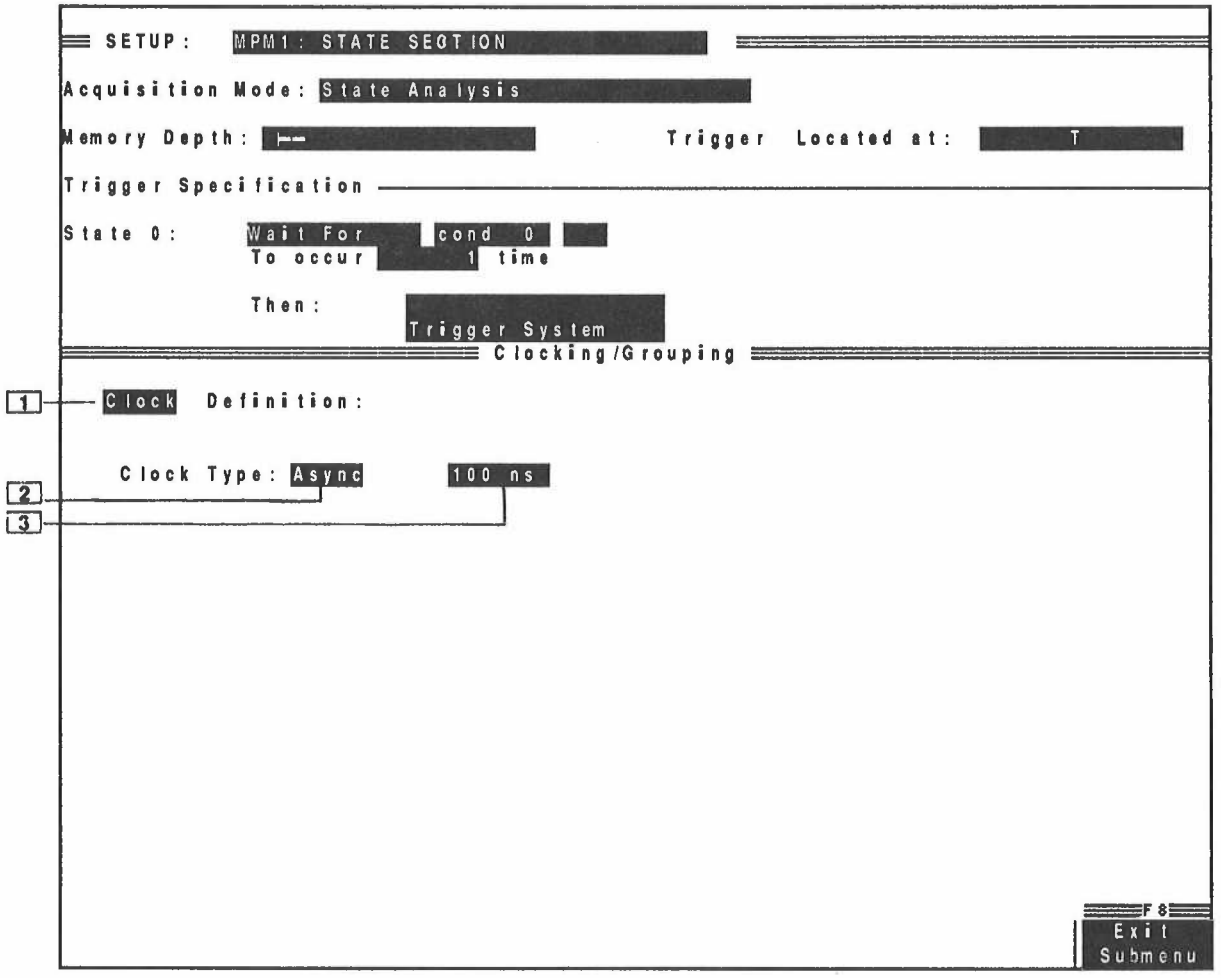


Figure 2-6. Clocking/Grouping submenu.

1 **Definition.** Allows you to choose either Clock or Group.

2 **Clock Type.** Allows you to choose Sync, Async, or Demux.

3 **Clock Rate.** Allows you to choose the rate of the asynchronous clock.

Function keys

F8: Exit Submenu. Allows you to leave the Clocking or Channel Grouping submenu.

Async

In asynchronous mode, the analyzer samples data at regular intervals determined by the analyzer. You can select the frequency of sampling in the clocking rate field. Table 2-1 lists the asynchronous speeds available.

Table 2-1
ASYNCHRONOUS CLOCKING SPEEDS

Nanoseconds	Microseconds	Milliseconds
100 ns	1 µs	1 ms
200 ns	2 µs	2 ms
500 ns	5 µs	5 ms
	10 µs	10 ms
	20 µs	20 ms
	50 µs	50 ms
	100 µs	100 ms
	200 µs	200 ms
	500 µs	500 ms

To change the clocking speed, place the cursor on the Clock Rate field and press the SELECT keys to cycle through the choices shown in Table 2-1.

Sync

Clock / Qualifier lines are 0, 1, and 4.

In synchronous mode, the SUT clock determines when the sample points occur.

Clock Line. An input line that is edge-sensitive and can be connected to the SUT clock. A clock line can be combined with other clock and qualifier lines to define when the data sample points occur.

Qualifier Line. An input line that is level-sensitive and can be combined with other clock and qualifier lines to define when the data sample points occur.

Clock/Qualifier Line. A line that can be used either as a clock line or as a qualifier line.

The acquisition clock definition consists of eight lines. Three of these lines can be clocks or qualifiers. These clock/qualifier lines are 0, 1, and 4. The other five lines can only be qualifiers. When you use synchronous mode, you must connect at least one of the clock/qualifier lines to an SUT clock signal. Any of the three clock/qualifier lines which are not connected to a clock may be used as qualifiers along with the other five qualifier lines.

NOTE

Remember to connect at least one of the clock/qualifier lines to an SUT clock signal.

Figure 2-7 shows the synchronous clocking submenu. The three clock/qualifier lines are shown in the Clock row. The lines which can be used as qualifiers are shown in the Qualifier row.

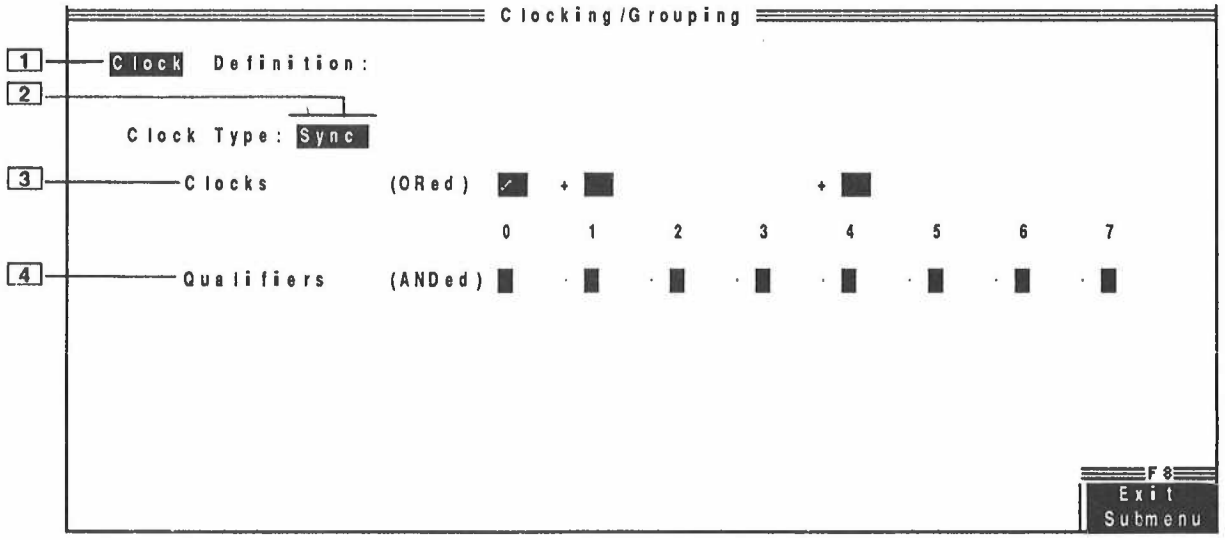


Figure 2-7. Synchronous Clocking submenu.

1 **Clock Definition.** Allows you to toggle between Clock and Grouping.

2 **Clock Type.** Allows you to choose Sync, Async, or Demux. In this case, Sync was chosen, for a synchronous acquisition clock.

3 **Clock row.** Choices which define the synchronous acquisition clock.

4 **Qualifier row.** Choices which qualify the synchronous acquisition clock.

Function keys

F8: Exit Submenu. Allows you to exit the Clocking submenu.

Only three lines can be used as clock inputs: 0, 1, and 4. There are four choices for defining valid input on a clock/qualifier line when it is used as a clock input: blank, rising and falling edges, rising edge, and falling edge. Table 2-2 shows the choices for clock input definitions.

Table 2-2
CLOCK DEFINITIONS

Symbol	When data is sampled
blank	data is not sampled; the clock line is ignored
X	at both the rising and the falling clock edges
/	at the rising clock edge
\	at the falling clock edge

To define a clock input, move the cursor to the field above the number representing the line you want to use as a clock. Use the SELECT keys to cycle through the choices in Table 2-2. The inputs from the clock row are ORed together. That is, if you are using multiple clock/qualifier inputs as clocks, the sampling clock is defined as any one of those lines achieving its defined sampling edge.

All the lines in the second row are the qualifiers. The qualifiers are ANDed together, and row is ANDed with the clock row to determine a valid acquisition clock cycle. Table 2-3 shows the qualifier definitions.

Table 2-3
QUALIFIER DEFINITIONS

Symbol	Qualifier Definition
blank	no qualification
0	logic low
1	logic high

To define a qualifier input, move the cursor to the field below the number representing the line you want to use as a qualifier. Use the SELECT keys to cycle through the choices listed in Table 2-3.

Setup and Hold Times

To guarantee that synchronously acquired data is properly sampled, the data must be stable (valid) around the clock edge. The terms used for the required time that data must be valid are setup time and hold time.

Setup time. The amount of time a signal must be valid *before* the clock edge occurs in order to be recognized.

Hold time. The amount of time the signal must be valid *after* the clock edge occurs in order to be recognized.

The setup time for a synchronous acquisition is 15 ns; the hold time is 0 ns. This means that when the active edge of a clock line

is found, the analyzer will check the value of all channels at some point between 15ns before the edge occurred and when the edge occurred. Because of the setup and hold requirements, some combinations of clock and qualifier choices create illegal options. For example, if you define clock line 0 as having a rising edge and define qualifier line 0 as having a 1, that situation can never be met. When the analyzer sees the rising edge on clock line 0, it does not have a positive hold time to look at the line and see that it has gone high.

When this happens a warning is displayed at the top of the screen, but you are not prevented from defining the clock illegally. There are some situations when you might want to be able to make an illegal definition, such as when a clock line also acts as a qualifier for a different clock line. For example, you can define clock line 0 with a rising edge and qualifier line 0 with a 1 if you have also defined another clock line for the analyzer to look at. In this case, when the second clock condition is met, qualifier line 0 may be high and the analyzer will have a valid clock.

Illegal combinations occur if you choose 0 or 1 as the qualifier for a rising and falling edge clock; 1 as the qualifier with a rising edge clock; or 0 as the qualifier with a falling edge clock. For easy reference, these combinations are shown in Table 2-4.

Table 2-4
ILLEGAL CLOCK AND QUALIFIER COMBINATIONS

Clock	Qualifier
X	0
X	1
⟋	1
⟍	0

Demux

In demultiplexed clocking, a two-phase sample is taken. You can set up two synchronous clocks to perform two-state clocking to allow you to acquire data from multiplexed lines, or from separate lines with alternating clocks.

In demultiplexing mode, a two-phase sample is taken: on the phase 1 clock pulse, some of the groups may be latched; on the phase 2 clock pulse, a second data sample is taken and both the phase 1 and phase 2 data samples are time-stamped and stored together. Figure 2-8 shows the demultiplexed submenu.

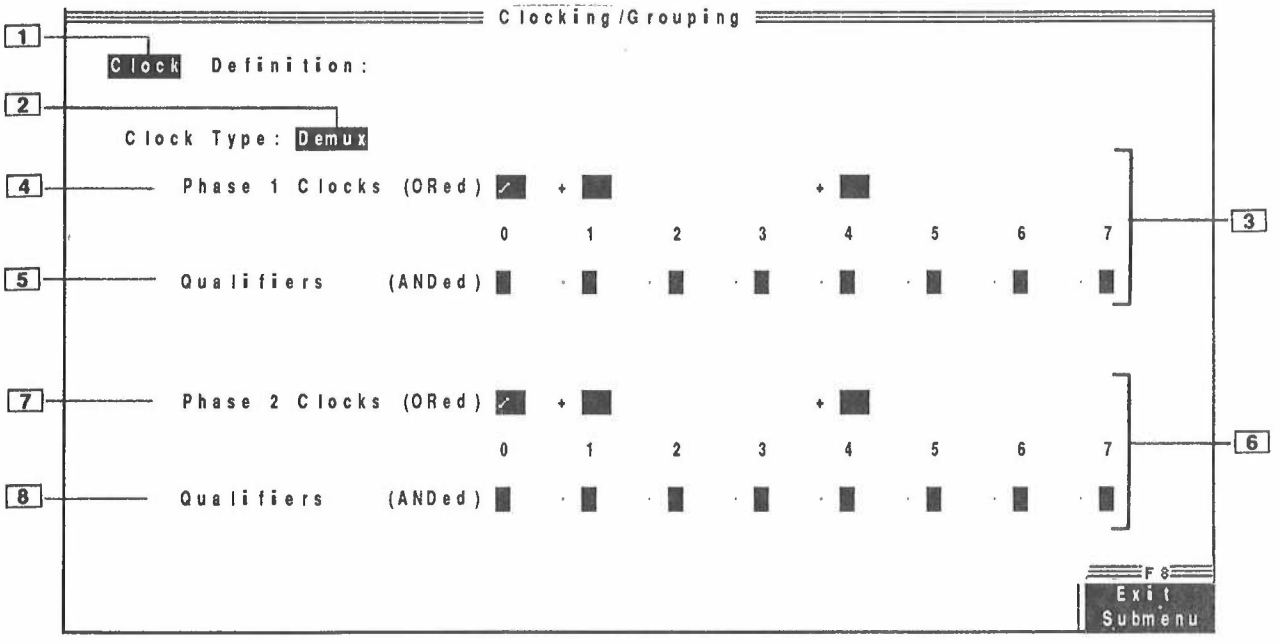


Figure 2-8. Demux Clocking submenu.

1 **Clock Definition.** Allows you to toggle between Clock and Grouping.

2 **Clock Type.** Allows you to choose Sync, Async, or Demux. In this case, Demux was chosen, for a demultiplexed acquisition clock.

3 **Phase 1 Definition.** Clock and qualifier definitions for the Phase 1 clock.

4 **Phase 1 Clock row.** Choices which define the Phase 1 synchronous acquisition clock.

5 **Phase 1 Qualifier row.** Choices which qualify the Phase 1 synchronous acquisition clock.

6 **Phase 2 Definition.** Clock and qualifier definitions for the Phase 2 clock.

7 **Phase 2 Clock row.** Choices which define the Phase 2 synchronous acquisition clock.

8 **Phase 2 Qualifier row.** Choices which qualify the Phase 2 synchronous acquisition clock.

Function keys

F8: Exit Submenu. Allows you to exit the Clocking submenu.

Each clock phase uses the same setup as the synchronous setup.

Choosing demultiplexing mode affects the channel groupings. Each group can be assigned to either the Phase 1 or Phase 2 clock. This is discussed in the Channel Groupings section.

Example: Setting up a demultiplexed clock definition. In this example eight bits of the data bus are multiplexed with eight bits of the address bus. In order to demultiplex the address and data information, double-probe these eight lines from the microprocessor. You can acquire data using two different sample clocks on these lines: one clock is valid when the data is present on the lines, the other clock is valid when the address is present on the lines.

You can use Phase 1 for the address. Since the microprocessor generates an Address Strobe when the address is valid, you can connect channel 0 to the address strobe line and define the Phase 1 clock as a rising edge on channel 0. In the channel grouping definition, the channel group used to show the address information is assigned to Phase 1.

You can use Phase 2 for the data. Since the microprocessor generates a data strobe when the data is valid, you can connect channel 1 to the data strobe line and define the Phase 2 clock as a rising edge on channel 1. In the channel grouping definition, the channel group used to show the data information is assigned to Phase 2. Figure 2-9 shows the clocking definition for this example.

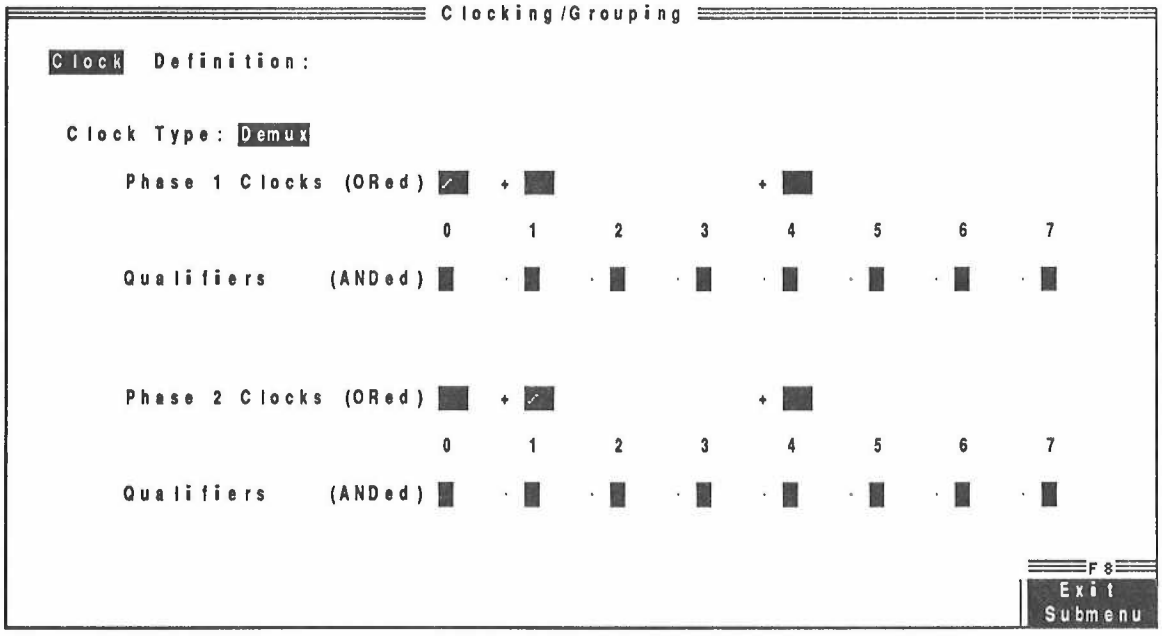


Figure 2-9. Demultiplexed clocking definition example.

When the microprocessor generates an address strobe, the probe will latch the signals for the Phase 1 group. When the microprocessor generates a data strobe, the probe will latch the signals for the Phase 2 group. At the Phase 2 clock, the logic analyzer will combine the groups together, timestamp them, and store them as a single bus cycle.

Press F8: Exit Submenu to exit this submenu and return to the State Section Setup menu.

Defining Channel Groups

Each lead to the SUT is a channel in the logic analyzer. Each is numbered 0 through 63 for the MPM module and 0 through 95 for the MPX module. Channels can be organized into meaningful groups which can be viewed in different radixes.

Channel. An input signal which is assigned a number by which you can identify each signal from the probe.

Group. An organization of a number of channels to form a meaningful combination, such as a 16-bit or 32-bit word.

You can assign channels to specific groups using the Clocking/Grouping submenu. From the State Section Setup

menu, press F6: Clocking/Grouping. Figure 2-10 shows the Channel Grouping submenu.

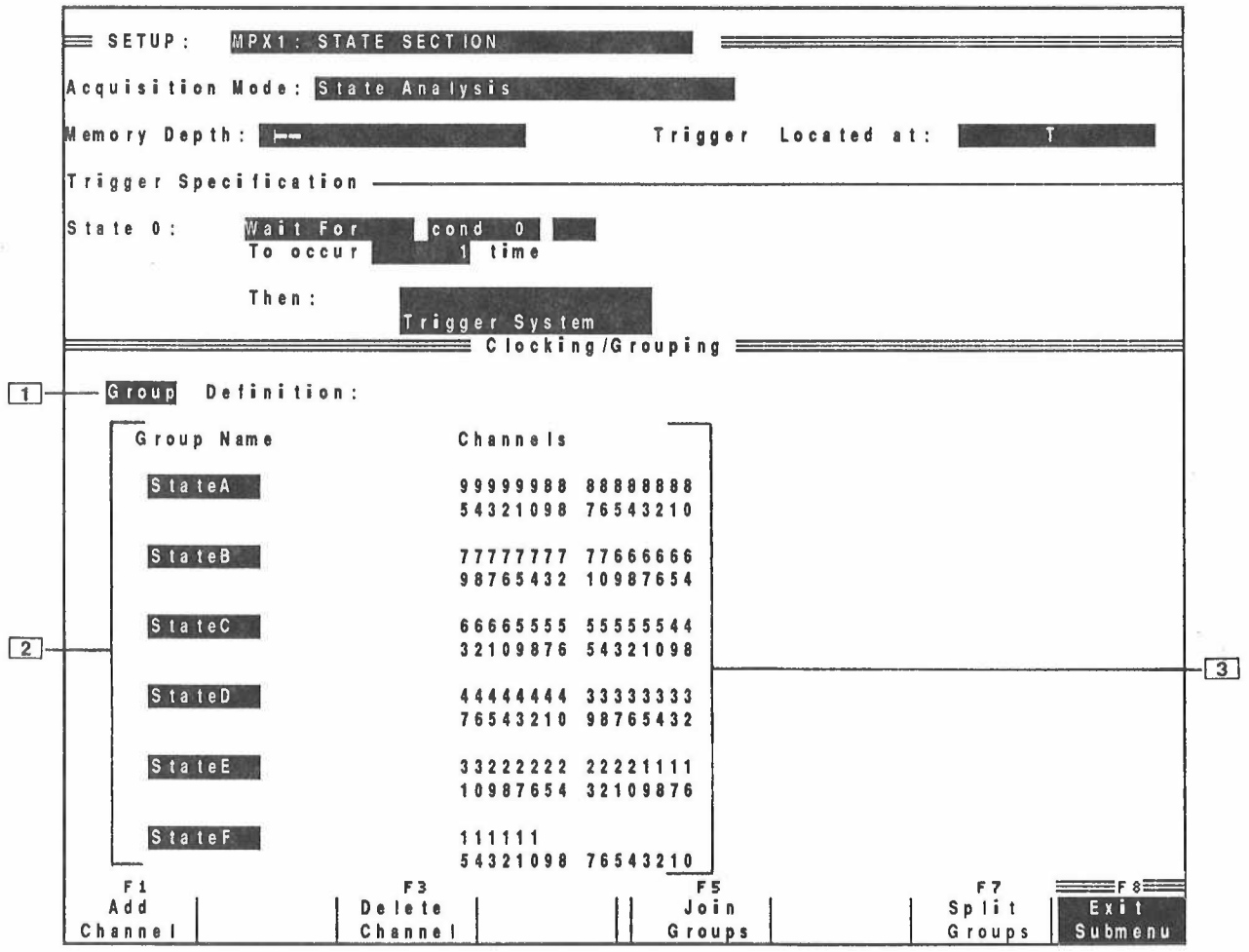


Figure 2-10. Channel Grouping submenu.

[1] **Group Definition.** Allows you to toggle between Clock and Grouping

[2] **Group Names.** Names which identify each particular group.

[3] **Channels.** Numbers which identify which leads are in which groups.

Function keys

F1: Add Channel. Allows you to add unassigned channels to a group.

F3: Delete Channel. Allows you to delete a channel from a group.

F5: Join Groups. Allows you to combine the current group with the next group.

F7: Split Groups. Allows you to divide a previously joined group into two groups.

F8: Exit Submenu. Allows you to exit the submenu.

You need to be aware of some channel grouping considerations before you connect probe leads to your system. The number of channels and groups available depends on whether you have a 30MPM or a 30MPX module. Table 2-5 lists the default channel-to-group assignments for each module.

Table 2-5
CHANNEL GROUPINGS

Module	Group	Channels
MPM	StateA	48-63
	StateB	32-47
	StateC	16-31
	StateD	0-15
MPX	StateA	80-95
	StateB	64-79
	StateC	48-63
	StateD	32-47
	StateE	16-31
	StateF	0-15

Channels 0, 1, and 4 are clock channels and channels 0 through 7 are qualifier channels. Clock and qualifier channels are set up in the Clocking submenu.

By default, the analyzer assigns channels to groups for you, but you can change these assignments. The default group size is 16 channels. Two contiguous groups may be joined, making a maximum of 32 channels per group.

NOTE

If you have an MPX application module, you cannot join StateC and StateD.

In forming your groups, use the highest numbered channel of your group for the most significant bit on the bus.

You can also change the names of the groups.

NOTE

While you may use up to eight characters to name a group, only the first six characters will appear in the State Table display.

You can rename a group by placing the cursor on the group to be renamed and entering the new name via the keyboard or keypad.

Deleting Channels From Groups

Use F3 to delete a channel from a group.

To delete channels from a group, move the cursor to the group and press F3: Delete Channel. Each time you press F3, the most significant channel in that group will be deleted. If you try to delete a channel from an empty group, you will get an error message telling you that there are no channels to delete.

Adding Channels To Groups

Use F1 to add a channel to a group.

To add a channel to a group, move the cursor to the group and press F1: Add Channel. Each time you press F1, the next sequential unassigned channel will be added to that group. If you press F1 when there are no unassigned channels available, you will get an error message telling you that all the channels are being used.

Joining Channel Groups

Use F5 to join two groups together.

To join two groups, place the cursor on a group (the first group) and press F5: Join Groups. The group below the first group (the second group) will be joined to the first group. If you have deleted channels from the second group, those channels will be restored to the second group with a message telling you that the deleted channels were restored. If channels have been deleted from the first group, those channels will still be deleted after joining with the second group.

Only two groups can be joined together. If you join two groups together and then try to join another group to that larger group, a message will appear telling you that you cannot join the two groups.

NOTE

If you have an MPX application module, you cannot join StateC and StateD.

Splitting Channel Groups

Use F7 to split a group.

After you have joined groups, you may split that large group back into two groups. Place the cursor on the group to be split and press F7: Split Groups. The analyzer will break the large group into the two original groups. If you try to split an original group, a message will appear telling you that you cannot split the group.

NOTE

In successive joining and splitting, if you have renamed any group, the new names will be maintained, but deleted channels will be restored.

If you have chosen demultiplexing mode for clocking, you can assign each group to either the Phase 1 or Phase 2 clock. Place the cursor on the Phase field and press the SELECT keys to toggle between the two phases.

Press F8: Exit Submenu to exit this submenu and return to the State Section Setup menu.

Defining the Trigger Specification

The Trigger Specification allows you to set up various conditions which must be satisfied before the analyzer will trigger.

Condition. A user-defined circuit event which the analyzer can recognize.

Test. The combination of conditions and subsequent actions.

State. The result of a test or combination of tests.

Action. Instructions which the analyzer must carry out when a test is satisfied.

The main component of Trigger Specification is the test. You can put conditions together to form a test. You can put tests together to form a state. As a result of a test, the analyzer performs various actions. Combinations of tests, states, and conditions can be put together to form multi-level triggering with a variety of actions attached to each level. Figure 2-11 shows a graphic representation of the relationship between these components.

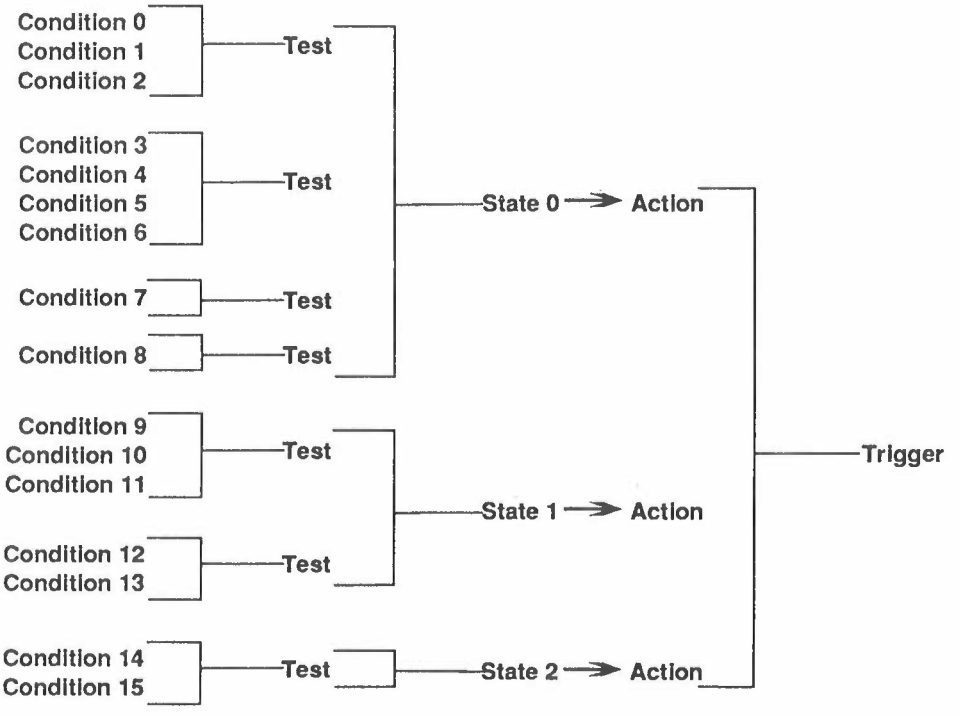


Figure 2-11. Representation of the relationship between elements of the Trigger Specification.

You can define up to eight tests.

You can use up to four conditions to form a test. You can put one or more tests together to form a state. You can define up to eight tests and up to seven states. As a result of a test, the analyzer performs various actions.

NOTE

If global storage qualification is being used, you can only define seven tests.

Combinations of tests, states and conditions can be put together to form multi-level triggering with a variety of actions attached to each level.

Figure 2-12 shows the State Section Setup menu with conditions put together to form a test and a state.

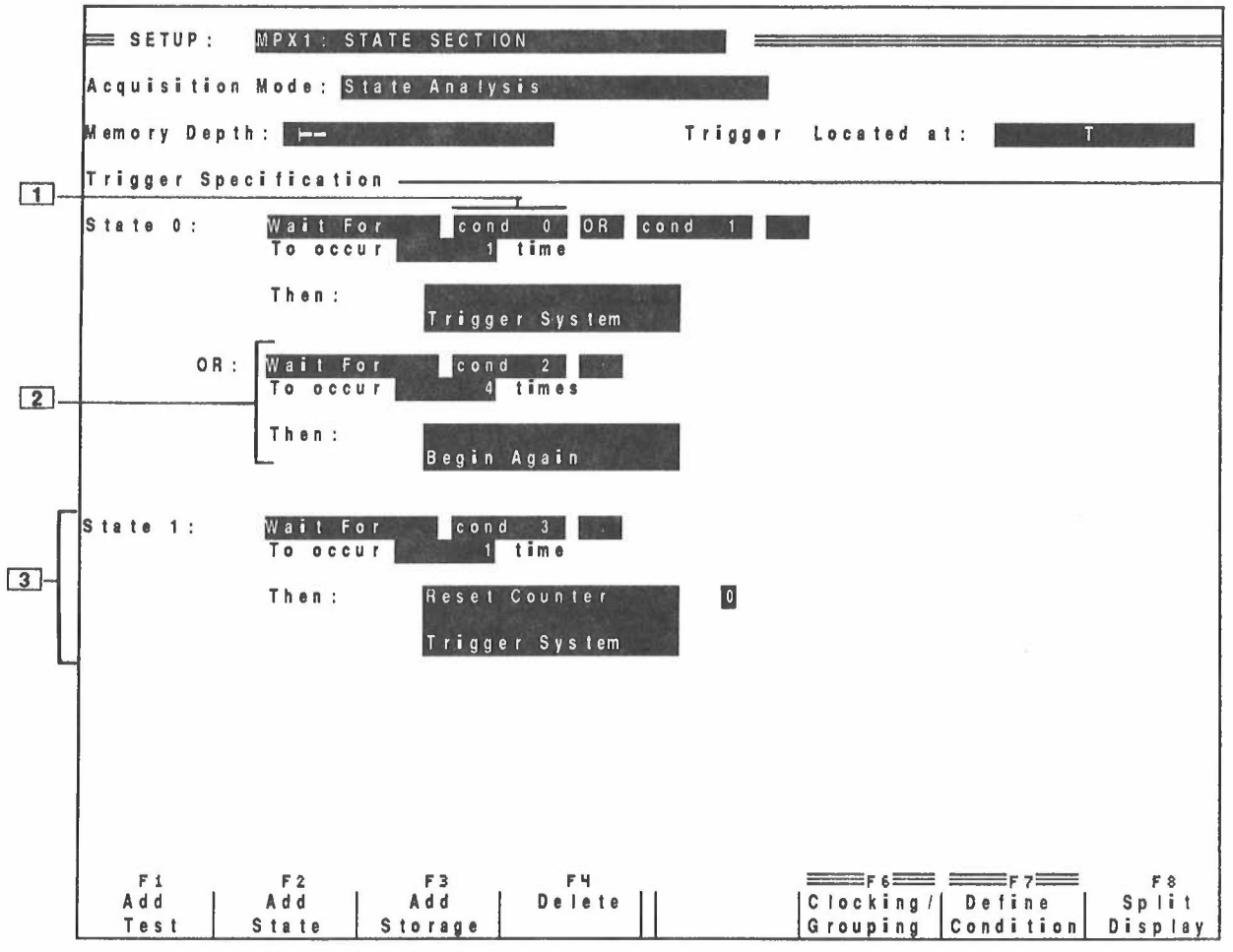


Figure 2-12. State Section Setup menu showing conditions, tests, and states.

1 **Condition.** A user-defined event which the analyzer can recognize.

2 **Test.** The combination of a condition and an action.

3 **State.** The result of a test or combination of tests.

Function keys

F1: Add Test. Allows you to add another test to the state where the cursor is located.

F2: Add State. Allows you to add another state to the trigger specification.

F4: Delete. Allows you to delete an element of the trigger specification.

Defining Trigger Conditions

Trigger conditions are specific circuit events that you can define. The analyzer can then recognize and test for them. In addition to circuit conditions, the analyzer can also keep track of time elapsed between two events, count the number of times a particular event occurs, and use a signal to communicate with other modules or module sections. Defined trigger conditions are incorporated in the trigger specification to cause the analyzer to perform various actions based on the conditions that occur.

Use F7 to define a condition.

You can define trigger conditions in the Define Condition submenu, which you access by pressing F7: Define Condition in the State Section Setup menu. Four types of conditions are available:

- **Word Recognizer.** Defines a word or range in any of four radixes.
- **Counter.** Counts the number of occurrences of defined events.
- **Timer.** Measures the amount of time between two events.
- **Signal.** Looks for a high or a low signal which was sent from another module or module section.

Figure 2-13 is a composite of two screens to show you one of each type of condition in the Define Condition submenu.

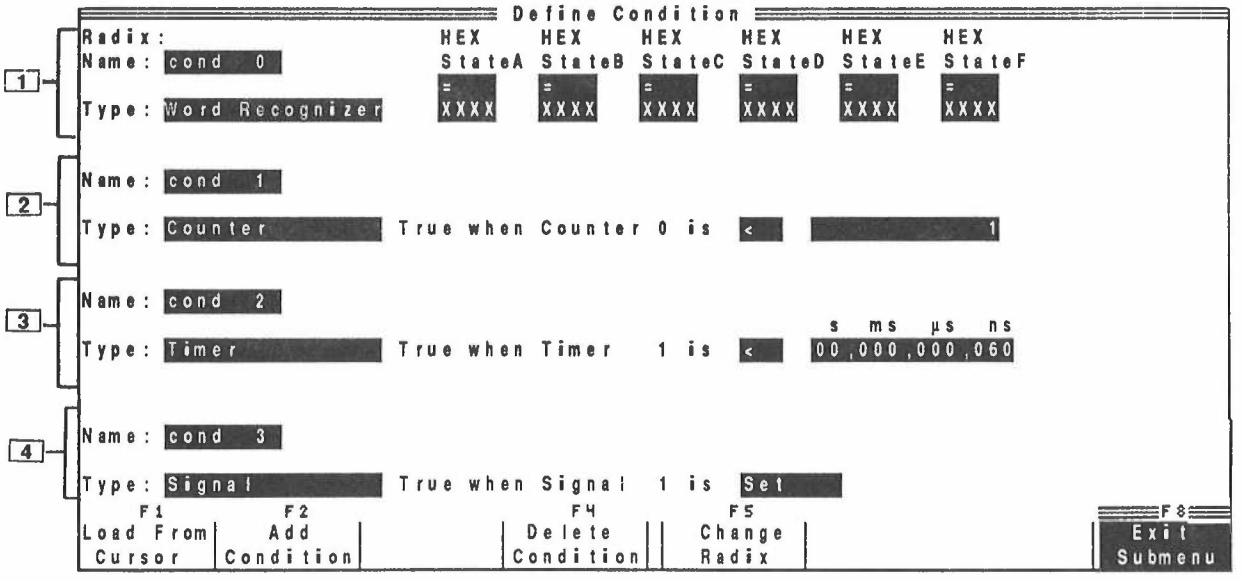


Figure 2-13. Define Conditions submenu.

[1] **Word Recognizer condition.** Allows you to define a word value or range of values in any of four radixes.

[2] **Counter condition.** Allows you to count the number of occurrences of defined events.

[3] **Timer condition.** Allows you to measure the amount of time between two events.

[4] **Signal condition.** Allows you to look for a high or low signal from another module or module section.

Function keys

F1: Load From Cursor. Allows you to use the value at the data cursor location in the display to define a word recognizer condition.

F2: Add Condition. Allows you to define a new condition.

F4: Delete Condition. Allows you to delete a condition.

F5: Change Radix. Allows you to choose the radix: BINary, OCTal, HEXadecimal, or SYMBOL.

F8: Exit Submenu. Allows you to exit the submenu.

You can define up to 20 conditions.

Use F2 to add a condition.

You can define a maximum of 20 conditions. The maximum number of counters and timers together is eight. That is, you can have any combination of timers and counters as long as the total number of conditions in the two groups combined does not exceed eight. The maximum number of word/range recognizer conditions is eight. The maximum number of signal conditions is four. Press F2: Add Condition to add a condition.

Use F4 to delete a condition.

You can delete conditions by moving the cursor to the condition you want to delete and pressing F4: Delete Condition. You cannot delete the last remaining condition. If you press F4 when there is only one condition, you will see an error message telling you that you cannot delete all the conditions.

Use F5 to change a word recognizer group's radix.

By default, the conditions are named Cond 0 through Cond 19. You can change the name of a condition by placing the cursor on the condition name and entering a new name using up to eight characters. If you rename a condition, and then delete it, the name you have given it will be lost. If you add that condition later, you have to rename it again.

To choose a type of condition, place the cursor on the Type field for the condition. Press the SELECT keys to cycle through the four choices.

Word Recognizer

You can define a data word or range composed of any or all of the channel groups which you defined in the Clocking/Grouping submenu. Refer to Figure 2-14 to see the fields pertaining to the word recognizer condition.

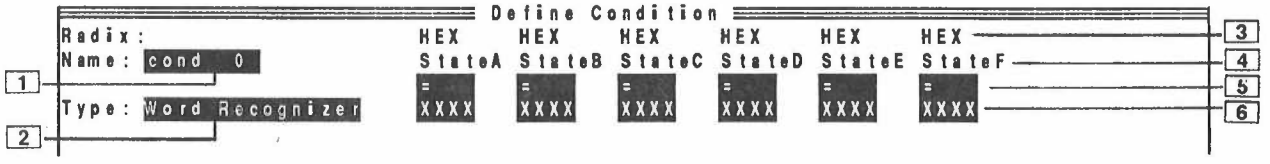


Figure 2-14. Word Recognizer Condition.

[1] **Condition Name.** Allows you to change the name of the condition.

[2] **Condition Type.** Allows you to choose between word recognizer, counter, timer, or signal.

[3] **Radix.** Shows you the radix: BINary, OCTal, HEXadecimal, or SYMBOL.

[4] **Group Name.** Shows you the channel grouping.

[5] **Condition Test Symbol.** Allows you to change the test symbol to define the relationship between the word (or words) and the data.

[6] **Value.** Allows you to enter a value for the word or the values for the upper and lower limits of a range.

The default value for the word recognizer fields is all Xs (Don't Cares), expressed in hexadecimal radix. You can cycle through the four choices of radix (Binary, Octal, Hexadecimal, and Symbol) by placing the cursor on any group definition and pressing
F5: Change Radix. For more information about using symbol as a radix, see the section *Using Symbols* in your system user's manual.

After you choose the radix, you can use the keyboard or keypad to enter any value for each group. Above the value for each group is a condition test symbol that you can use to precisely define the relationship between the word you are defining and the data against which the trigger will test. There are four choices. Table 2-6 shows the symbol of each choice and what it means in relation to the word being defined.

Table 2-6
WORD RECOGNIZER CONDITION TEST SYMBOLS

Symbol	Name	Condition true or satisfied when
=	Equal	Acquired data is exact match for defined word.
≤	Less than or equal to	Acquired data is less than or equal to word.
≥	Greater than or equal to	Acquired data is greater than or equal to defined word.
≤=≤	Within range	Acquired data is within the range defined by the two words.

When Within range is selected, two values for the word in that group can be defined, the first one for the beginning value of the range, the second one for the ending value of the range. The beginning value must be less than the ending value or the results are indeterminate. If either of the two values have an X (Don't Care) for a channel, the same channel will be treated as X in the other value.

You can fill in values from the data cursor location using the Load From Cursor function. Place the cursor on a word recognizer condition. Press F1: Load From Cursor. The condition value will become the data value that the active cursor in the display is on.

Counter

Counters are used to keep track of the number of times particular events occur. Counters are incremented by actions in the Trigger Specification definition.

You can define up to eight counters.

You can define up to eight counters, as long as the total number of counters and timers together does not exceed eight. Counter/timer conditions are numbered 0 through 7. See Figure 2-15 for the counter condition fields.

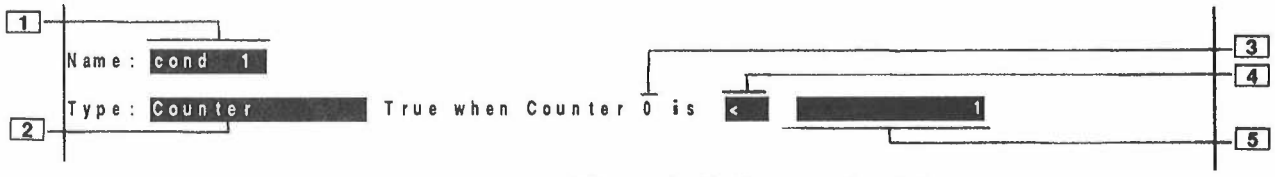


Figure 2-15 Counter Condition.

1 **Condition Name.** Allows you to change the name of the condition.

2 **Condition Type.** Allows you to choose between word recognizer, counter, timer, or signal.

3 **Counter Number.** Shows you which of eight counters this condition is.

4 **Condition Test Symbol.** Allows you to change the test symbol to define the relationship between the counter comparison value and the actual counter value.

5 **Counter Comparison Value.** Allows you to enter a comparison value for the counter.

Each counter is defined the same way. The test is true when the condition is satisfied. Table 2-7 shows the counter condition test symbols and their meanings.

Table 2-7
COUNTER CONDITION TEST SYMBOLS

Symbol	Meaning
<	less than
≥	equal to or greater than

The analyzer compares the number the counter has reached with a number you define in the value field. This can be any number between 1 and 2,147,483,647. Comparisions can only be made within this range, but the counter can continue counting up to 17,592,186,044,415. To view the total count, use the Auxiliary Data submenu in the State Table display. For information about the Auxililary Data submenu, refer to the section *Displaying Data* in your system user's manual.

Timer

You can define up to eight timers.

Timers are used to measure time between or during events. Timers are started and stopped by actions in the Trigger Specification definition. You can define up to eight timers, as long as the total number of counters and timers together does not exceed eight. Counter/timer conditions are numbered 0 through 7. See Figure 2-16 for the timer condition fields.

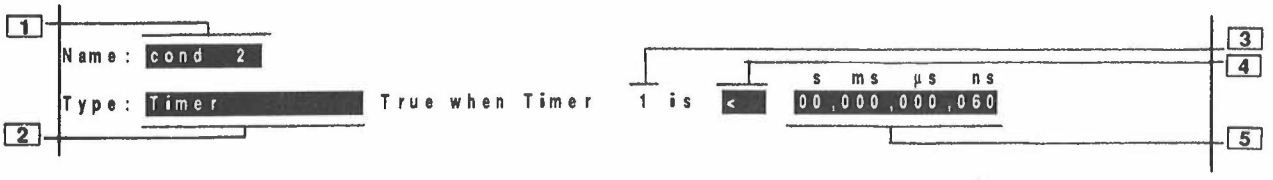


Figure 2-16. Timer Condition.

1 **Condition Name.** Allows you to change the name of the condition.

2 **Condition Type.** Allows you to choose between word recognizer, counter, timer, or signal.

3 **Timer Number.** Shows you which of eight timers this condition is.

4 **Condition Test Symbol.** Allows you to change the test symbol to define the relationship between the timer comparison value and the actual timer value has reached.

5 **Timer Comparison Value.** Allows you to enter a comparison value for the timer.

Each timer is defined the same way. The test is true when the condition is satisfied. Table 2-8 shows the timer condition test symbols and their meanings.

Table 2-8
TIMER CONDITION TEST SYMBOLS

Symbol	Meaning
<	less than
≥	equal to or greater than

The analyzer compares the timer value to the time you define in the value field. The time range is between 60 nanoseconds and 42.949,672,960 seconds. The time value can be any value within this range in 20-nanosecond increments. Comparisions can only be made within this range, but the timer can continue timing up to 97 hours, 44 minutes, 3.720,888,360 seconds. To view the total time, use the Auxiliary Data submenu in the State Table display. For information about the Auxililary Data submenu, refer to the section *Displaying Data* in your system user's manual.

Signal

You can define up to four signal conditions.

The signal condition is used to identify signals from another module or module section in the PRISM system. The condition checks for a logic high or logic low on a specified line from another module. You can define up to four signal conditions. See Figure 2-17 for the names of the signal condition fields.

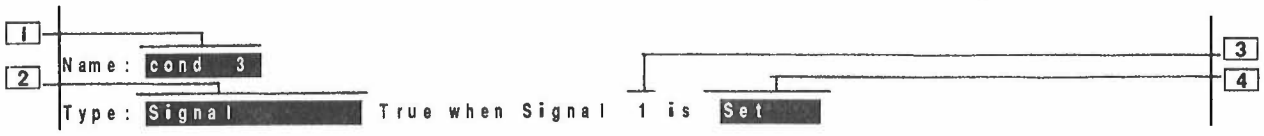


Figure 2-17. Signal Condition.

1 **Condition Name.** Allows you to change the name of the condition.

2 **Condition Type.** Allows you to choose between word recognizer, counter, timer, or signal.

3 **Signal Number.** Shows you which of four signals this condition is.

4 **Signal Value.** Allows you to choose Set (logic high) or Clear (logic low).

The signal conditions are numbered 1 through 4. Each signal condition is defined the same way. The analyzer compares the status of a specified line (high or low) with the signal value you

define in the value field (set or clear). The value field can be Set for logic high or Clear for logic low.

A signal that has been set by the State Section can also be used as a condition in the State Section Trigger Specification. In this way a signal can be used as a flag.

Defining a Test

The test is the main component of the Trigger Specification. A test consists of a condition test line, an occurrence number, and an action. See Figure 2-18 to see a test and the names of the fields related to a test.

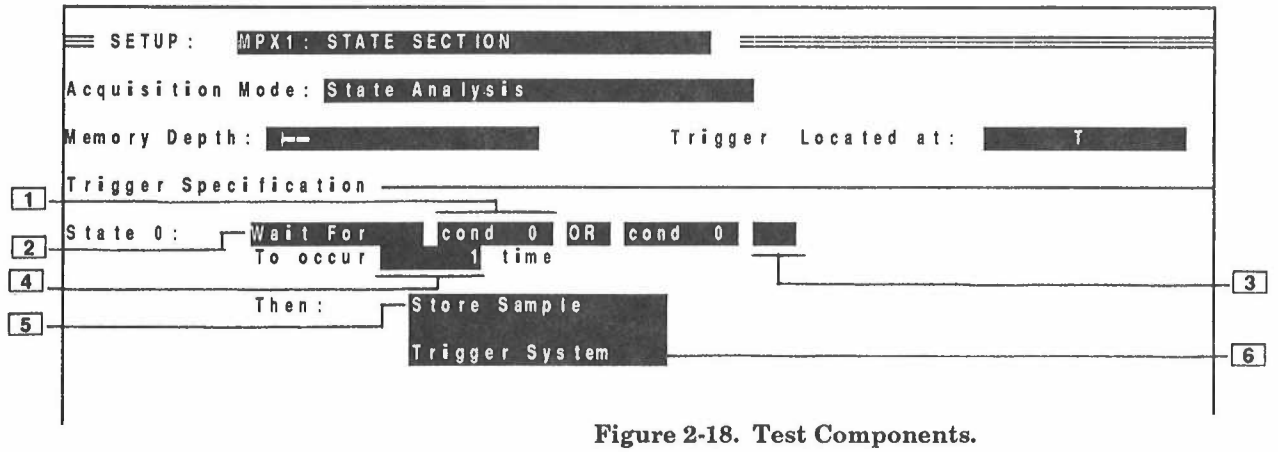


Figure 2-18. Test Components.

1 **Condition.** Allows you to choose which condition is involved in the test.

2 **Condition Test.** Allows you to choose Wait For (Not) or If (Not).

3 **Boolean Operator field.** Allows you to choose AND or OR when using more than one condition.

4 **Occurence Number.** Allows you to choose how many times the condition must be met before the action takes place.

5 **General Action.** An optional instruction for the analyzer to perform if the test is met.

6 **State Control Action.** A mandatory instruction for the analyzer to perform if the test is met.

You can use up to four conditions in a test.

The condition test line can have up to four test conditions. Each condition used in the trigger setup must be defined in the Define Condition submenu.

NOTE

Remember to define conditions before using them in the trigger setup.

You must use the same Boolean operator on all the conditions in the same line.

If there are multiple conditions in the test, they are linked with ANDs or ORs. You must use the same Boolean operator on all the conditions in the same line. You cannot AND some conditions and OR others.

The conditions may be tested in two basic ways:

- **Wait For (Not).** The test is combined with the occurrence number and results in an action.
- **If (Not).** The test results in one of two actions: the Then action or the Else action.

The occurrence number is used with Wait For (Not) and indicates the number of times the condition test must be true before the action will be taken. The range of the occurrence counter is between 1 and 65,535. If the occurrence value is 1, the test will be true every time the condition is satisfied. When using an occurrence value other than 1, the test will be true only while the count is equal to the value.

NOTE

Occurrences can only be counted with a Wait For (Not) test.

The If (Not) adds the element of an alternative action. When the condition is true, the Then action is taken; when the condition is false, the Else action is taken.

Use the SELECT keys with the cursor on the blank box at the end of the line to add a condition.

To add a condition to the condition test, place the cursor on the blank box at the end of the line and press the SELECT keys. Another condition will be added, joined by an OR. You can change the OR to an AND by moving the cursor to the Boolean Operator field and pressing the SELECT keys.

Use F4 to remove a condition from a test.

To remove a condition from the test, move the cursor to the condition to be deleted and press F4: Delete. The condition the cursor was on will be deleted.

Adding a Test

Use F1 to add a test.

You can add a test to a state by pressing F1: Add Test. The new test will be added below the cursor location. If you have more than one test in a state, they must be the same type. That is, all tests in one state must be Wait For or Wait For Not or all the tests in one state must be If or If Not.

If there are multiple tests defined in a state and more than one of them are satisfied at the same time, only the actions of the first satisfied test will be performed.

NOTE

A Wait For (Not) test will increment its occurrence counter and will no longer be true on the next acquisition cycle.

Use F4 to delete a test.

You can delete a test by moving the cursor to the condition test in that state to be deleted and pressing F4: Delete. The test the cursor was on will be deleted.

Adding a State

Use F2 to add a state.

You can add a state by pressing F2: Add State. The new state will be inserted below the cursor position on the screen. You can define a combination of up to seven states. States are numbered 0 to 6.

NOTE

The number of states available is limited by the number of tests being used.

Use F4 to delete a state.

You can delete a state by moving the cursor to the state to be deleted and pressing F4: Delete. The analyzer will display a message asking for confirmation. If you wish to delete the state, perform the appropriate action as described in the message. The states which follow the deleted state will be renumbered so there is no gap in state numbering.

Defining Actions

There are two kinds of actions: state control actions and general actions. State control actions tell the analyzer what to do next. Each test must have one state control action. General actions are optional. Each test can have no general actions or one or more general actions.

State Control Action. A mandatory instruction for the analyzer to perform if the test is met.

General Action. An optional instruction for the analyzer to perform if the test is met.

State Control Actions

There must be one, but no more than one, state control action in each test.

State control actions tell the analyzer what to do next. There must be one state control action in each test. There cannot be more than one state control action in each test. There are five state control actions:

- **Trigger Section.** When the condition is satisfied, the State Section triggers. All counters and timers are stopped and storage qualification remains unchanged.
- **Trigger System.** When the condition is satisfied, all active modules in the system trigger (if they haven't already triggered). All counters and timers are stopped and storage qualification remains unchanged.
- **Begin Again.** When the condition is satisfied, the State Section returns to the state it was in when Start was pressed: all active counters and timers are set to 0 and operation restarts at State 0.
- **Go To State *n*.** When the condition is satisfied, on the next cycle go to the state specified by *n*. If you specify an undefined state an error message will appear. Going to another state clears all occurrence counters. You may want to specify going to the current state in order to clear the occurrence counters.
- **Do Nothing.** When the condition is satisfied, the analyzer will remain in the current state. You might want to use this in conjunction with one or more general actions.. Since this action does not clear the occurrence counters, you might use this while you wait for a counter, timer, or occurrence counter to reach a specified value.

You cannot delete the state control action.

You can change the state control action by placing the cursor on the state control action of the test and pressing the SELECT keys to cycle through the five choices. You cannot delete the state control action.

General Actions

General actions control the timers and counters, set and clear intermodule signals, and turn state section storage on and off. By default, storage is on. There are 11 general actions:

- **Store Sample.** Stores the acquisition sample.

- **Start Storage.** Begin to store all data samples including the current sample.
- **Stop Storage.** Stop storing data samples after the current sample. Global storage qualification may still cause some samples to be stored.

NOTE

If Store Sample, Start Storage, Stop Storage is used anywhere in the trigger specification, or Global Storage Specification is turned on, storage will be turned off at the beginning of the acquisition. If no storage is specified, all data samples will be stored.

- **Set Signal *n*.** Send a high signal, number *n*, to other modules in the PRISM. You can only select a signal that is currently used in a condition definition. You can have up to four intermodule signals, numbered 1 through 4.
- **Clear Signal *n*.** Send a low signal, number *n*, to other modules in the PRISM. You can only select a signal that is currently used in a condition definition. You can have up to four intermodule signals, numbered 1 through 4.
- **Reset Counter *n*.** Change the value of counter *n* to 0. You can only select a counter that is currently used in a condition definition. You can have up to eight counters, numbered 0 through 7.
- **Increment Counter *n*.** Add 1 to the value of counter *n*. You can only select a counter that is currently used in a condition definition. You can have up to eight counters, numbered 0 through 7.
- **Restart Timer *n*.** Reset timer *n* to 0 and start timing. You can only select a timer that is currently used in a condition definition. You can have up to eight timers, numbered 0 through 7.
- **Resume Timer *n*.** Turn timer *n* on and resume timing from the current accumulated time value. You can only select a timer that is currently used in a condition definition. You can have up to eight timers, numbered 0 through 7.
- **Stop Timer *n*.** Turn timer *n* off. The current accumulated time value is maintained. You can only select a timer that is currently used in a condition definition. You can have up to eight timers, numbered 0 through 7.

- **Assert Stop Line.** Generate a user-selectable pulse on the Stop line of a PDT 30RPI probe. This is only used by the Prototype Debug Tool. For information about the PDT, refer to section *Using the Prototype Debug Tool* in this manual.

Use the SELECT keys with the cursor on the blank action line to add a general action.

You can add a general action by placing the cursor on the blank line above the state control action and pressing the SELECT keys to cycle through the ten choices.

Use F4 to delete a general action.

You can delete a general action by placing the cursor on the general action to be deleted and pressing F4: Delete. The general action will be deleted, leaving the blank line above the state control action.

Defining Global Storage Qualifications

Use F3 to add or to delete storage qualification.

Global Storage qualification is a conditional test conducted independently of the storage instructions in the trigger specification which you can apply to your data to decide whether or not the data should be stored. You can define Global Storage qualifications by pressing F3: Add Storage. See Figure 2-19 to see the Global Storage qualification fields.

NOTE

Turning on Global Storage qualification changes the default in the Trigger Specification from ***Storage On*** *to* ***Storage Off****. If you want to acquire datea and store it while using Global Storage, you must explicitly do so by including* ***Store Sample*** *in your Trigger Specification.*

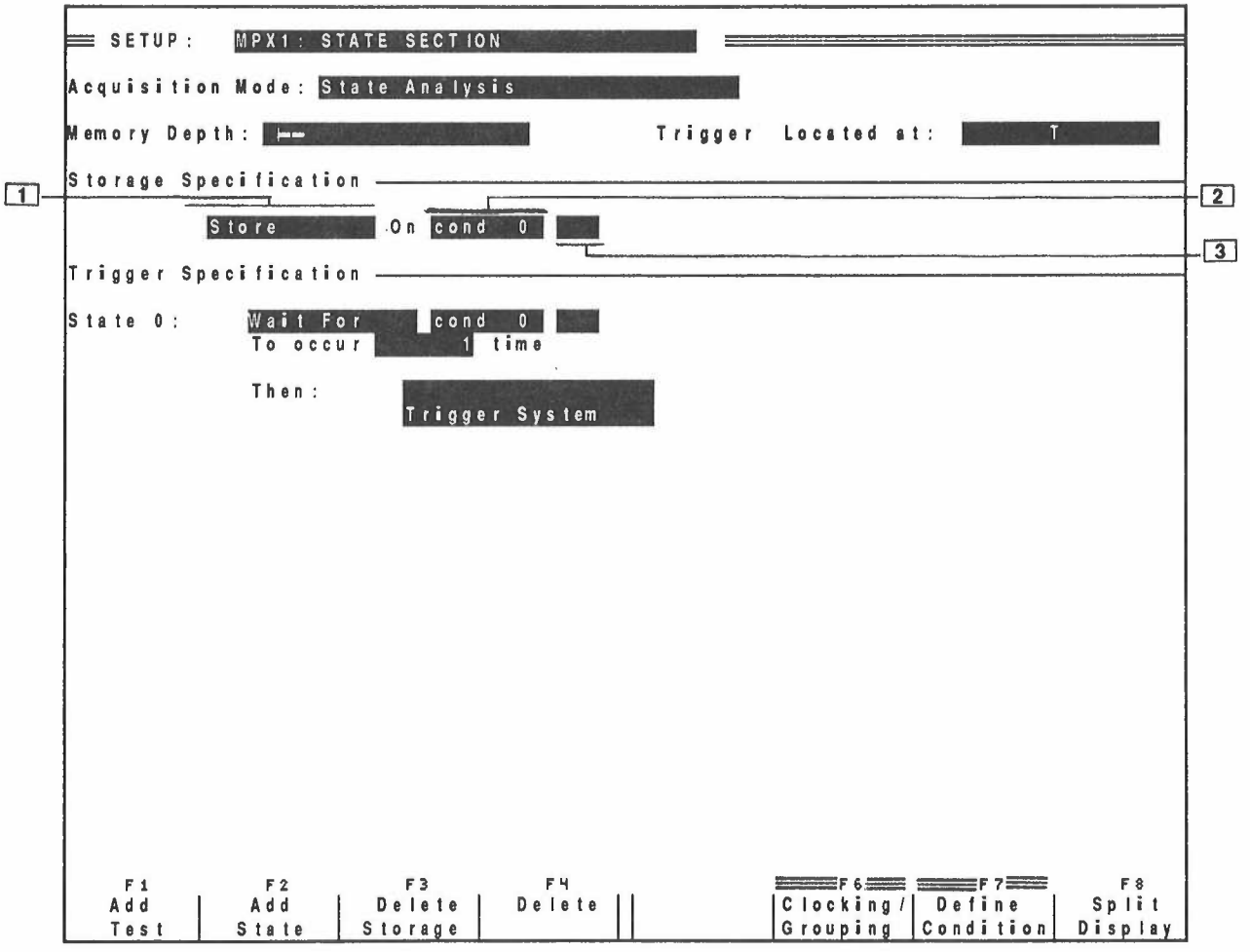


Figure 2-19. Global Storage Qualification fields.

1 **Global Storage Action.** Allows you to choose Store or Do Not Store.

2 **Storage Condition.** Allows you to choose the condition to be met.

3 **Boolean Operator field.** Allows you to choose AND or OR when using more that one condition.

Function keys

F3: Delete Storage. Allows you to turn off Global Storage specification.

You can use up to four conditions in the Storage Specification.

The Storage Specification line consists of a storage action and up to four conditions. Each condition used in the trigger setup must be defined in the Define Condition submenu.

If there are multiple conditions on the conditions line, they are linked with ANDs or ORs. You must use the same Boolean operator on all the conditions in the same line. You cannot AND some conditions and OR others.

There are two storage actions:

- **Store.** If the condition is satisfied, the analyzer will store the data.
- **Do Not Store.** If the condition is satisfied, the analyzer will not store the data.

If the condition is true, the analyzer stores the data sample. If the condition is false, the analyzer will not store.

If you have defined a test under Trigger Specification which includes Store Sample, Start Storage, or Stop Storage, the result of the test is ORed with the results of Storage Specification testing.

NOTE

Adding global storage specification makes one less test available for your use. If you have used the maximum number of tests you will not be able to use global storage unless you delete a test.

You can delete the storage specification by pressing F3: Delete Storage.

Making an Acquisition

After you have defined the trigger specification you are ready to make an acquisition.

Press the Start/Stop key. While the analyzer is acquiring data, the Acquisition Status screen is displayed. This screen keeps you informed of the progress of your acquisition. For information about the Acquisition Status display, refer to the section *Acquiring Data* in your system user's manual.

When the analyzer completes the acquisition, it immediately displays the data stored in the acquisition memory in the display format previously used. If the display has not been accessed since powering up, the default display is State Table.

If the analyzer cannot complete the acquisition, the Acquisition Status screen will remain on the display. Press the Start/Stop key again to complete the acquisition.

DISPLAYING DATA WITH THE STATE SECTION

When the analyzer has completed the acquisition, it automatically shows the State Table Display. You can view the data in state table format or as a timing diagram. To change display formats, place the cursor in the first field of the display menu and press the SELECT keys to cycle through the choices.

Various display features are available to you in State Table display and Timing Diagram display. For information on display features, refer to section *Displaying Data* in your system user's manual.

Section 3: USING THE TIMING SECTION

The Timing Section of the MPM application module functions independently of the State Section. The Timing Section samples data, searches for a trigger event, stores data, and performs an action. Nine single-threshold channels can be used to define one trigger event word. You can acquire data samples at a maximum rate of one sample every 5 ns (200 MHz).

Data from all acquisition channels can be stored in acquisition memory or reference memory to view and analyze. You can view Timing Section data samples in both State and Timing Display formats.

In order to use the Timing Section, you must make the following three connections:

1. Connect the P6486 timing probe to the mainframe.
2. Connect a timing leadset to the P6486 probe.
3. Connect the timing leadset to the SUT.

Descriptions of the probe and leadsets and their installation instructions follow.

P6486 Timing Probe

The P6486 probe is used to make an acquisition with the Timing Section.

Probe. The hardware that connects the mainframe to a leadset. The probe is usually composed of a connector to the mainframe, a cable, a plastic housing containing a circuit board, and a connector to the leadset.

Leadset. The hardware that connects the probe to the SUT. The leadset is usually composed of a connector to the probe, a plastic housing, which sometimes contains a circuit board, and cables or leads with connectors which attach to the SUT.

To connect the P6486 Timing Probe to the mainframe, insert the P6486 Timing Probe cable connector into the Timing Section panel connector on the mainframe. The Timing Section connector is the one closest to the front of the mainframe. This panel connector is keyed so that only the Timing Probe cable

connector will fit in it; the Timing Probe cable connector will only fit with the keying tabs at the top of the connector.

Press the button labeled ID on the probe for probe and leadset information.

To identify which MPM module the timing probe is connected to, press the button labeled "ID" on the P6486. The module or section number to which the timing probe is connected will be displayed on the top line of the screen. An example of such an ID number is "MPM1: Internal Probe 0 with 10/2 leadset". (The 10/2 leadset is the standard leadset.)

Leadsets

The Timing Section has two different leadsets that you can use: the standard leadset and the high performance leadset.

The Standard leadset has 10 signal and two reference leads.

The standard leadset (also called the 10/2 leadset) comes with your P6486 and is suitable for most timing situations. The standard leadset has 10 signal leads (color coded by channel number, see Table 3-1) and two reference leads (labeled REF).

Ground. A 0 V condition, usually the reference from which system voltages are measured.

Reference. A voltage from which system voltages are measured. Usually this is ground, or 0 V.

The High Performance leadset has 10 signal leads, each with its own reference lead.

The high performance leadset (also called the 10/10 leadset) is suitable for use in faster timing situations. The high performance leadset has 10 signal leads, each with its own reference.

NOTE

The high performance leadset is recommended for monitoring high speeds.

Refer to Figure 3-1 and the following procedure while connecting a standard or high performance leadset to your SUT, the leadset to the P6486 Timing Probe, and the P6486 to the Timing Section panel connector of your PRISM 3000 Series mainframe.

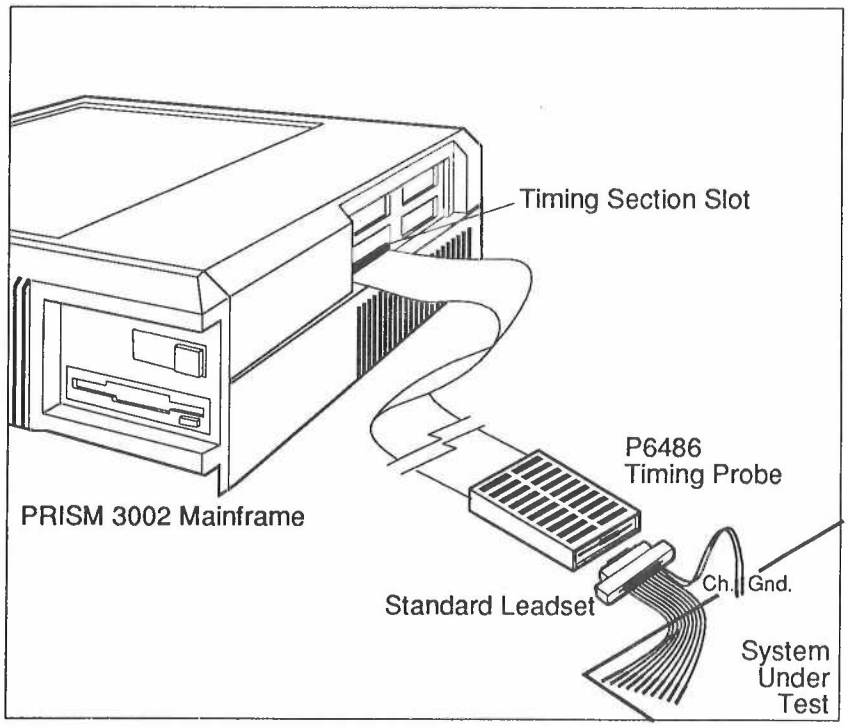


Figure 3-1. Connecting the P6486 Timing probe.

1. Attach the channel leads to the SUT. The standard leadset has 12 leads. The reference leads are the first and last green leads and the other 10 leads are color coded using resistor color code values to indicate channel number-to-color assignment as shown in Table 3-1.

Table 3-1
STANDARD LEADSET COLOR CHANNEL NUMBER

Color	Channel Number
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8

The high performance leadset has 10 podlets, each with a channel contact and a reference contact. The podlets are identified on the leadset label according to channel number. You can use a reference/signal lead set (Tektronix part number 196-2963-00) to to allow use of standard grabber tips (Tektronix part number 020-1386-01, package of 12), if needed.

You can use a reference/signal lead set (Tektronix part number 196-2963-00) to to allow use of standard grabber tips (Tektronix part number 020-1386-01, package of 12), if needed.

You must attach channel 9 to the clock of your SUT when operating in the Synchronous Acquisition mode. You cannot acquire any data on channel 9 of either leadset when used with the MPM Timing Section.

2. Attach the reference leads to the SUT. The first and last leads (both green) are reference on the standard leadset. The channels and references on the high performance podlets are marked as such.

GETTING STARTED USING THE TIMING SECTION

This section will show you how to acquire data using the Timing Section, the P6486 Timing probe, the standard leadset, and the FasTrak circuit board that came with your mainframe. For demonstration purposes, there are two examples presented: a simple acquisition using transitional mode and an acquisition using transitional mode showing bursts of data.

Example 1: Transitional Acquisition Mode

This example shows you how to make a simple acquisition using the transitional acquisition mode. You will connect the MPM to the SUT, change the Timing Section setup menu, and acquire data. You will view the data in the timing display format and observe that all the channels change edges simultaneously. You will then observe through closer examination that the channels are actually changing edges in a staggered fashion.

In this example, the FasTrak circuit board functions as the SUT. Perform the following steps to connect the mainframe to the FasTrak:

1. Connect the P6486 timing probe to the mainframe according to the instructions listed under P6486 Timing Probe earlier in this section.
2. Connect the standard or the high performance leadset to the P6486 probe according to the instructions listed under Leadsets earlier in this section.
3. Connect the leadset to the FasTrak circuit board pins according to Table 3-2. Refer to Figure 3-2 for the location of counter/timer pins, ground pins, and power connection on the FasTrak circuit board.

Table 3-2
MPM CONNECTIONS FOR EXAMPLE 1

Standard Leadset Channel Number and Color	FasTrak Counter/Timer Pin Names
Channel 8 (gray)	3 KHz
Channel 7 (violet)	6 KHz
Channel 6 (blue)	12 KHz
Channel 5 (green)	24 KHz
Channel 4 (yellow)	48 KHz
Channel 3 (orange)	97 KHz
Channel 2 (red)	195 KHz
Channel 1 (brown)	390 KHz
Channel 0 (black)	781 KHz
Reference (2) (green)	Ground

Channel 9 is only used for synchronous acquisitions.

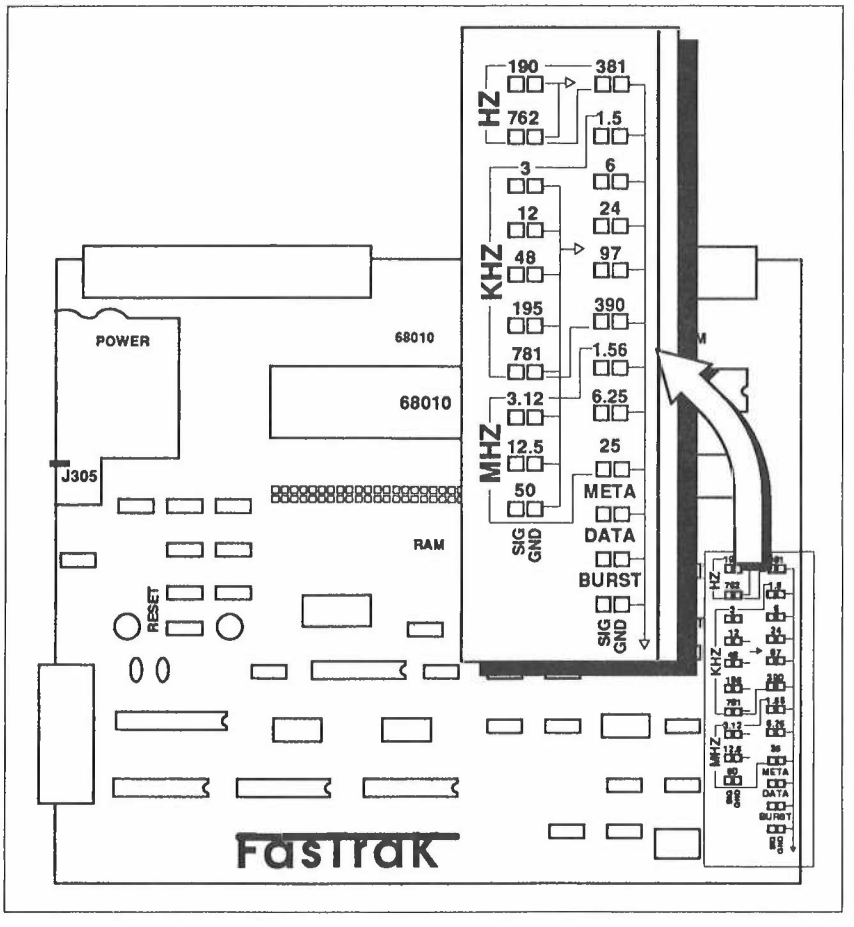


Figure 3-2. FasTrak circuit board pin locations.

Use the following steps to set up the MPM:

1. Power on the mainframe.
2. Access the State Section setup menu and select Off for the acquisition mode.
3. Access the Timing Section setup menu and change the following:
   a. The trigger position should be at the start of memory (T in the left-most position).
   b. The True/False event field should be set to True.

After completing the connections and setup, you can acquire timing data. Follow these steps to acquire data from the FasTrak board:

1. Plug one end of the FasTrak's power supply into an outlet and the other end into the +5 V connector, J305, on the FasTrak circuit board.
2. Press Start on the mainframe.

   After you press Start, the mainframe displays information on the status of the trigger test. When the analyzer detects the first transition on any channel, it marks that location as the trigger, and displays data in State Table display format when the acquisition is 100% complete.
3. Access the Timing display menu to view the data in Timing Diagram display format.
4. Change the Time per Division field to 1 µs.

   Your data should resemble that shown in Figure 3-3. Move your cursor to any data sample where all the channels appear to rise or fall simultaneously. Refer to your mainframe user's manual for information regarding how to move the cursor and scroll through data.

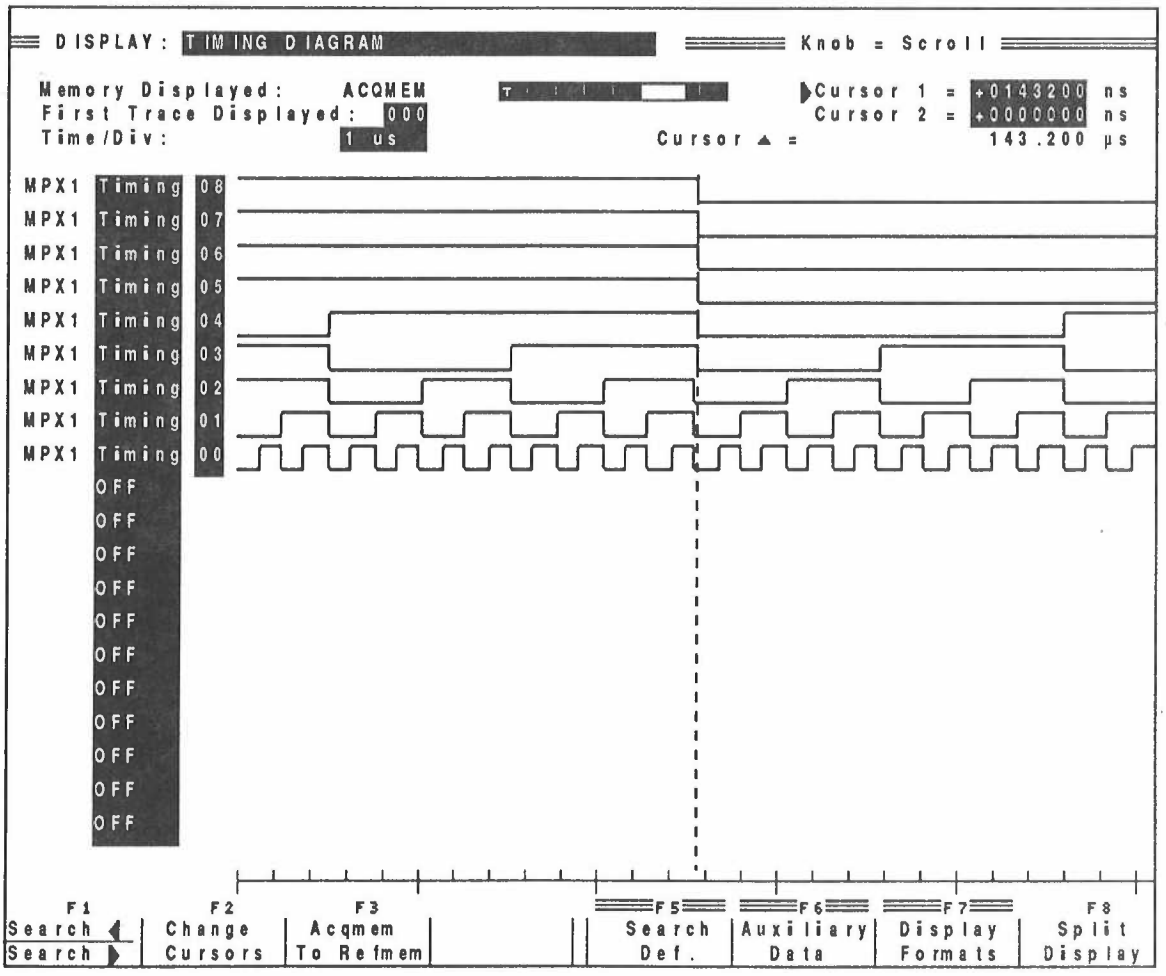


Figure 3-3. Plain transitional acquisition data. This view shows timing data at 1 µs per division.

5. Change the Time per Division field to 10 ns. At this greater magnification you can see that the channels are not changing edges simultaneously at all. Instead, they are changing edges with a 10 ns to 15 ns skew. This variance is because slight time delays occur between ICs and components on the FasTrak board. Figure 3-4 shows how the same data looks at 10 ns per division.

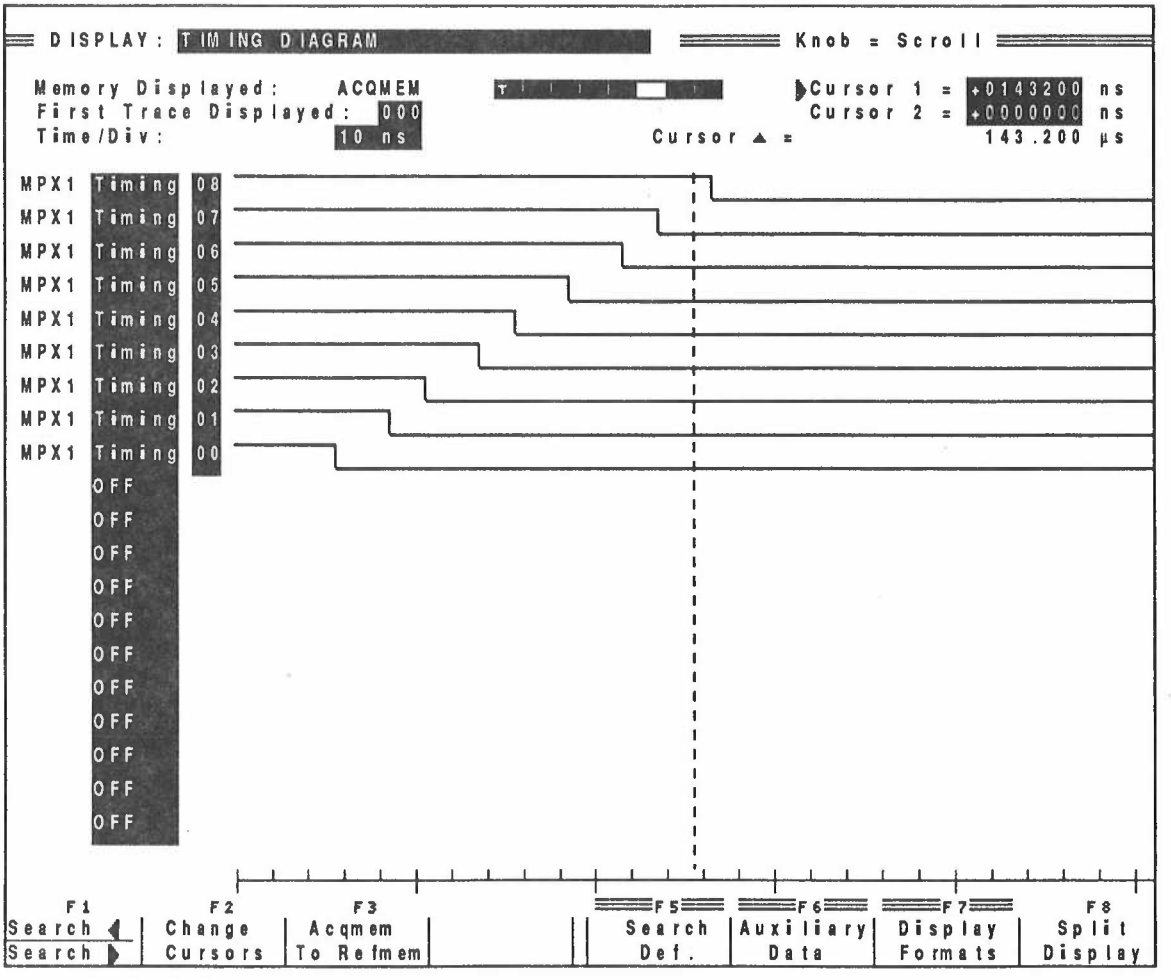


Figure 3-4. Magnified plain transitional acquisition data. This view shows the same timing data as in Figure 3-3 at 10 ns per division.

Example 2: Transitional Acquisition Mode Showing Bursts of Data

This example shows you how to acquire bursts of data using the transitional acquisition mode. You will connect the MPM to the SUT, change the Timing Section setup menu, and acquire data. You will view the data in the timing display format and observe several bursts of data on channel 8. You will then observe that what appears to be a single burst of data is actually four groups of eight 10 ns data bursts each.

In this example, the FasTrak circuit board is again the SUT. Perform the following steps to connect the mainframe to the FasTrak:

1. Connect the P6486 timing probe to the mainframe according to the instructions listed under P6486 Timing Probe earlier in this section.
2. Connect the standard or the high speed leadset to the P6486 probe according to the instructions listed under Leadsets earlier in this section.
3. Connect the leadset to the FasTrak circuit board pins according to Table 3-3. Again, refer to Figure 3-2 for the location of counter/timer pins, ground pins, and power connection on the FasTrak circuit board.

Table 3-3
MPM CONNECTIONS FOR EXAMPLE 2

Standard Leadset Channel Number and Color	FasTrak Counter/Timer Pin Names
Channel 8 (gray)	Burst
Channel 7 (violet)	190 Hz
Channel 6 (blue)	381 Hz
Channel 5 (green)	762 Hz
Channel 4 (yellow)	Ground
Channel 3 (orange)	Ground
Channel 2 (red)	Ground
Channel 1 (brown)	Ground
Channel 0 (black)	Ground
Reference (2) (green)	Ground
Channel 9 is used as CLK in synchronous acquisitions.	

Use the same steps you used in Example 1 to set up the MPM.

After completing the connections and setup, you can acquire timing data. Follow these steps to acquire data:

1. Plug one end of the FasTrak's power supply into an outlet and the other end into the +5 V connector, J305, on the FasTrak circuit board.
2. Press Start on the mainframe.

   After you press Start, the mainframe displays information on the status of the trigger test. When the MPM finds the first transition on any channel, it marks that location as the trigger, and displays data in State display format when the acquisition is complete.

3. Access the Timing display menu to view the data in timing display format.
4. Change the Time per Division field to 1 ms. Your data should resemble Figure 3-5. Note the burst of activity on channel 8 that occurs about every 5.25 ms.

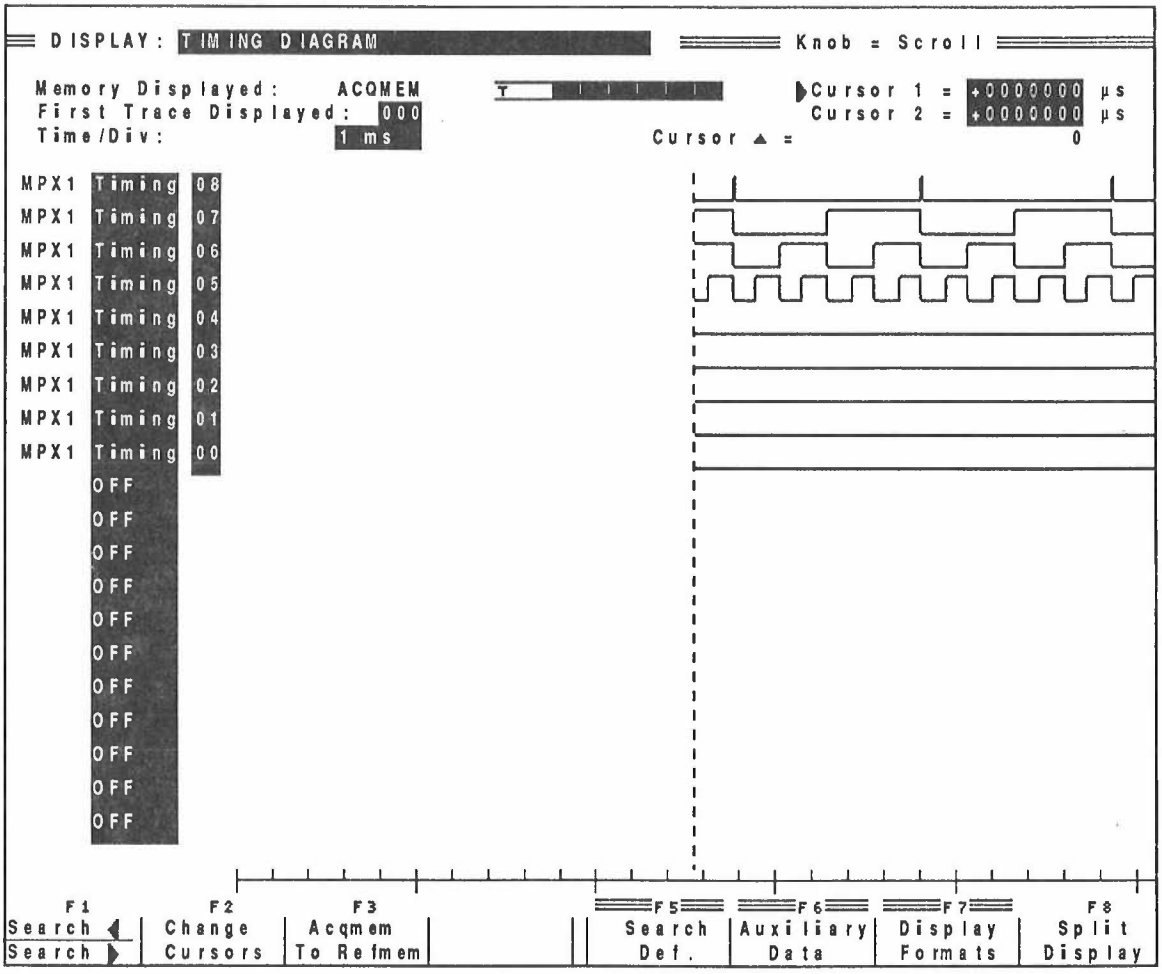


Figure 3-5. Data bursts captured using transitional acquisition mode.

5. Press F8: Split Display to view the data in a split screen display. Change the lower screen to display the Timing Display menu.
6. Change the Time per Division field to 1 ms in the lower screen. Position the active cursor on the first data burst (at the extreme left of the display).

7. Change the Timer per Division field to 10 µs to magnify the data burst. Reposition the active cursor on the data burst and change the Timer per Division field to 100 ns to greater magnification. Your data should resemble Figure 3-6. Notice that what appears as a signal burst in the upper screen now appears as separate bursts in the lower screen.

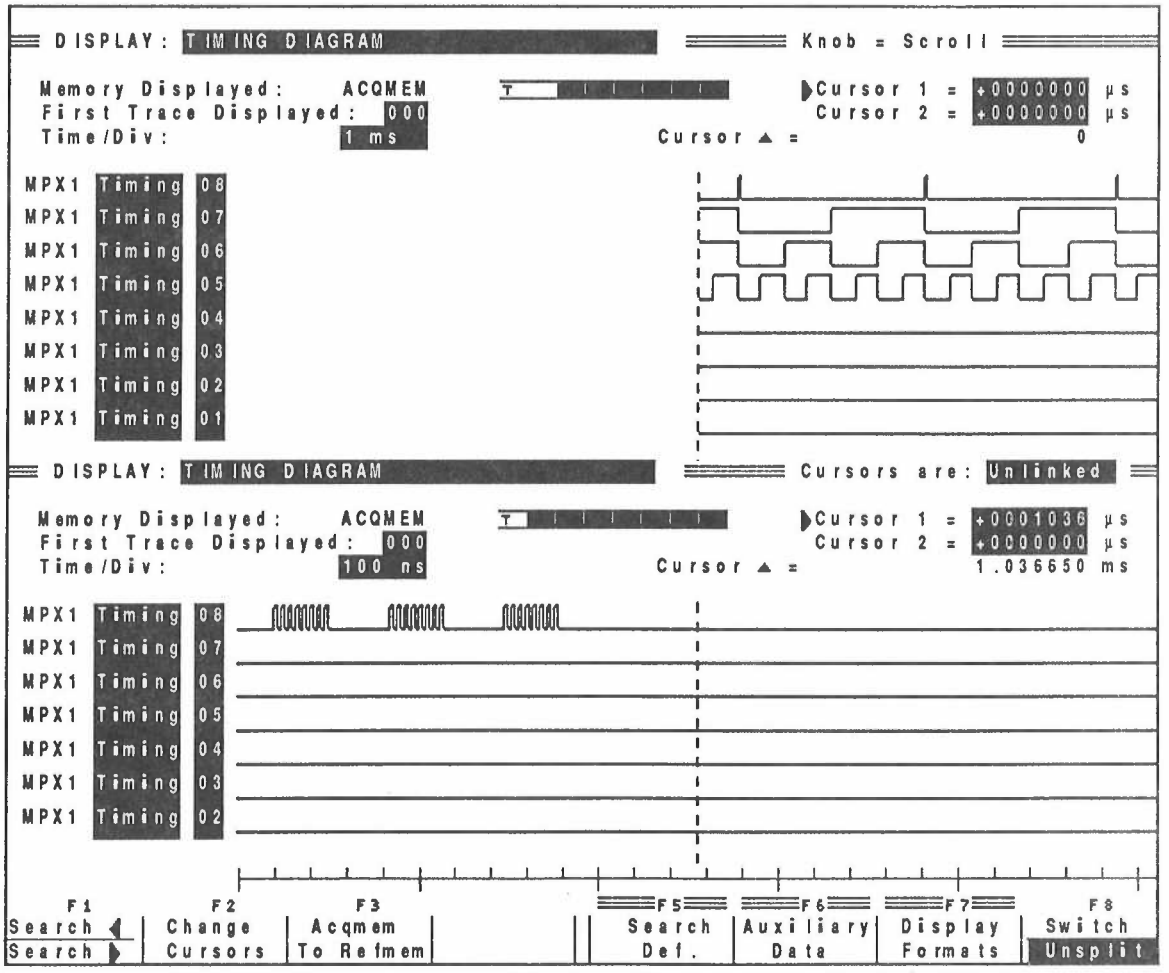


Figure 3-6. Magnified data burst using split screen. What appears as a single data burst in the u pper screen appears as several data bursts in the lower screen.

8. Again, reposition the active cursor on one of the data bursts in the lower screen. Change the Timer per division field to 10 ns. Your data should resemble Figure 3-7. Under greater magnification, you can see that one of the four bursts viewed in the last step consists of a series of pulses.

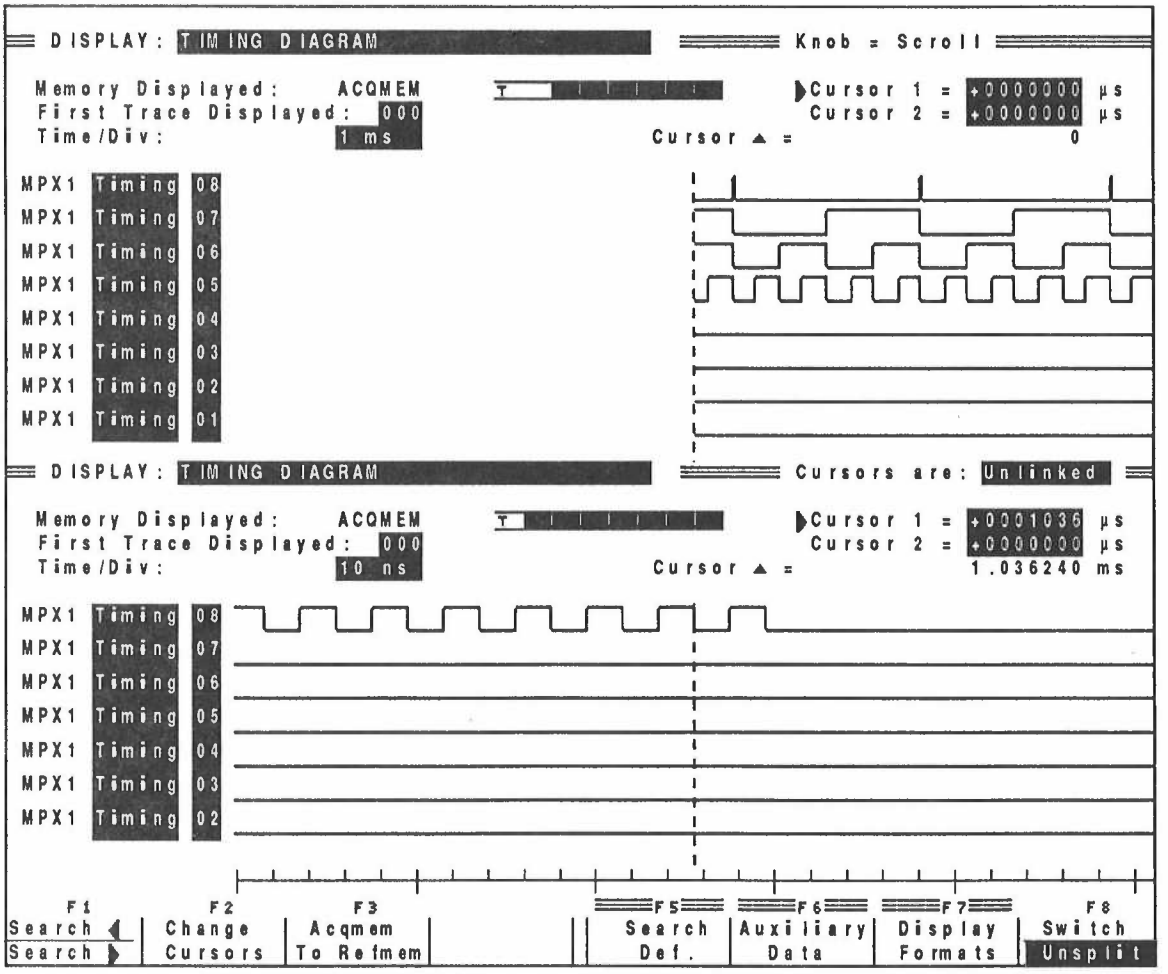


Figure 3-7. Fully-magnified data burst. One of the bursts in the lower screen of Figure 3-6 is magnified to show that it consists of a series of pulses.

ACQUIRING TIMING DATA

The Timing Section setup menu allows you to specify the data to acquire and store. To set up the Timing Section for acquisition, you must define the following in the Timing Section:

- acquisition mode
- trigger position in memory
- acquisition threshold voltage
- channel groups (through the Channel Grouping submenu)
- trigger event
- communication links with other modules and module sections

To access the Timing Section setup menu, press the Setup key and scroll through the setup menu choices until you reach the Timing Section. You will have more than one Timing Section setup menu if you have more than one MPM installed in your system. Refer to the mainframe user's manual for a description of how modules such as the MPM are identified.

A default setup allows you to acquire data using the Timing Section. To modify the default setup and acquire Timing Section data, follow these steps:

1. Connect the P6486 Timing Probe to the MPM timing slot, the leadset (standard or high performance) to the P6486, and the flying leads of the standard leadset or the podlets of the high performance leadset to the system under test (SUT). For detailed information about making these connections, refer to the sections *P6486 Timing Probe* and *Leadsets* earlier in this section.
2. Specify the following in the Timing Section setup menu:
   a. Select the acquisition mode.
   b. Define the logic threshold voltage level.
   c. Press F6: Channel Grouping submenu to group channels.
   d. Select to trigger the logic analyzer (system) or Timing Section.
   e. Choose to set a signal to interact with one or more modules or sections.
3. If you wish, select another module or section setup menu and make the appropriate selections as needed.
4. Press Start, Auto, or Cont to begin acquiring data.

If you press Start/Stop before the trigger event is found, the Timing Section halts acquisition and displays STOP at the end of acquisition memory.

Figure 3-8 shows the Timing Section setup menu, briefly describes each field, and lists the available selections. The remainder of this section discusses the selections in more detail.

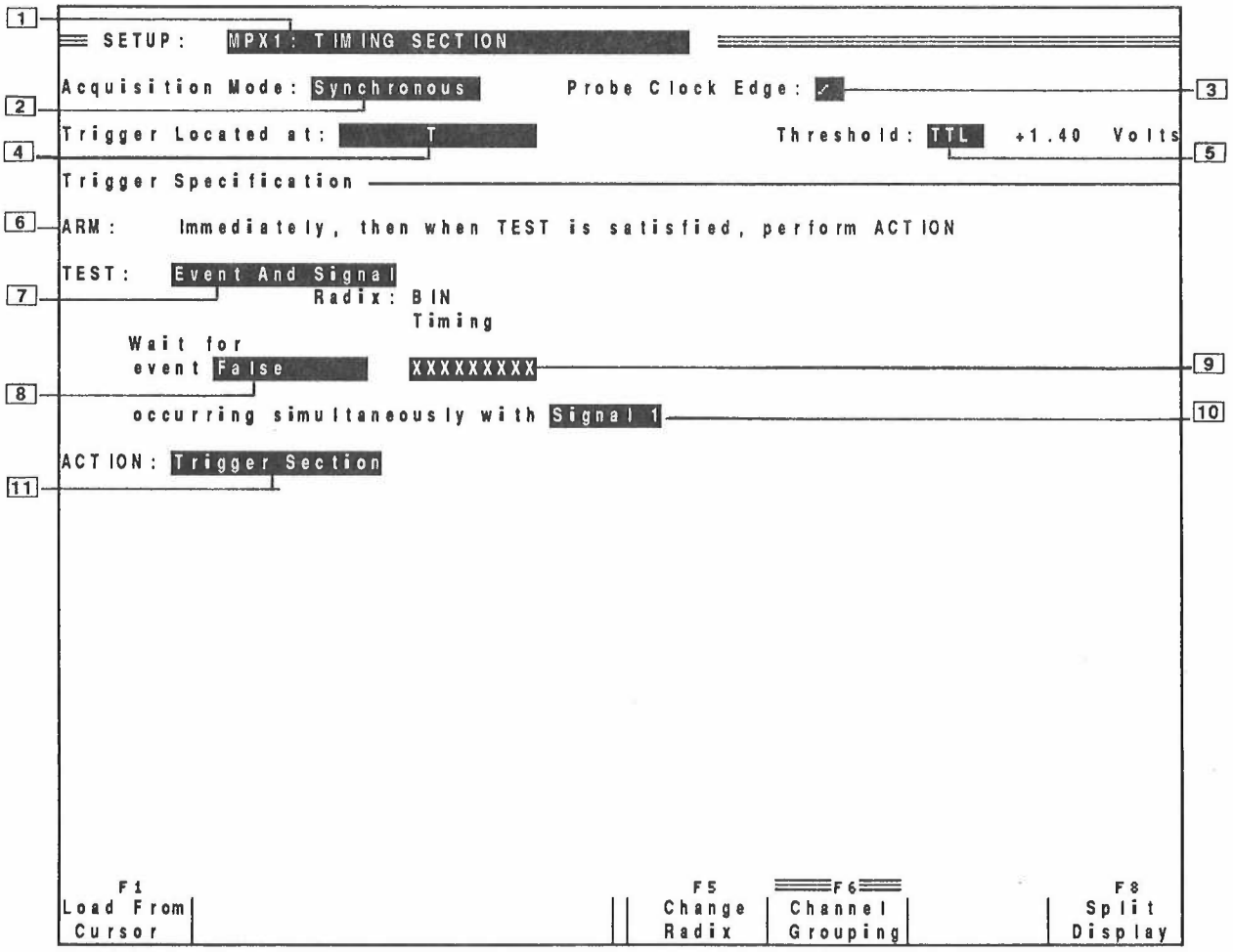


Figure 3-8. Timing Section setup menu.

[1] **Menu Select.** Lets you select a menu from the setup menu group.

[2] **Acquisition Mode.** Lets you select the source of the acquisition clock for data sampling. Selections are Synchronous, Transitional, and Off.

[3] **Probe Clock Edge.** This field is only available when the Synchronous Acquisition Mode is selected. Lets you acquire data on either the rising or falling edge of the clock channel to which the leadset is connected.

[4] **Trigger Position.** Determines the amount of data stored after the trigger. Five trigger positions are offered.

[5] **Threshold.** Lets you specify the logic threshold voltage. Selections are TTL, ECL, CMOS, and VAR (variable). Variable threshold allows you to enter a value from +10 V to -10 V in increments of 50 mV for the standard leadset

and a value from +5 V to -5 V in increments of 25 mV for the high performance leadset.

[6] **Arm.** Lets you specify to start searching for a trigger immediately or after a signal (1-4) is received from another module or section if you select to trigger on an event. If you select to trigger on Event And Signal, the Timing Section arms immediately.

[7] **Trigger Test Type.** Lets you define the trigger test as an Event or as an Event And Signal.

[8] **Trigger Event True/False.** Lets you specify whether to trigger when the trigger event is True or False.

[9] **Trigger Event.** Lets you enter a channel group value as the event to trigger on.

[10] **Signal In.** Lets you specify which signal must be true when the event is satisfied in order to satisfy the trigger condition. This field occurs only if Event and Signal is the trigger test selection.

[11] **Action.** Lets you specify an action for the logic analyzer to perform when the trigger event is found. Selections are Trigger Section, Trigger System, Trigger Section and Set Signal (1-4), and Trigger System and Set Signal (1-4).

Function Keys

F1: Load From Cursor. Loads the channel group value from the active data cursor in the display window. The field cursor must be positioned on a channel group value.

F5: Change Radix. Changes the radix for the channel group the field cursor is positioned on. Available radixes are binary, octal, hexadecimal, and symbol.

F6: Channel Grouping. Accesses the Channel Grouping submenu.

F8: Split Screen. Splits the screen horizontally. When you use the split screen display, this function key toggles to Switch/Unsplit.

Selecting the Acquisition Mode

You can use the acquisition mode to select the source of the acquisition clock for data sampling. You can select one of two types of acquisition modes in which to sample data: transitional or synchronous. You can also choose Off to turn the Timing Section off.

Transitional acquisition. An acquisition in which data sampling occurs each time any channel changes its logic level.

Synchronous acquisition. An acquisition in which the data sampling occurs each time the SUT clock pulses.

Transitional Acquisition Mode

Use transitional acquisition mode when you want a data sample each time a signal changes.

The simplest way to set up an acquisition from a SUT is to use the transitional acquisition mode. You can acquire data samples with a resolution of 5 ns from a SUT. The data rate on each channel is limited to 10 ns between transitions.

The transitional acquisition mode can extend the effective memory depth of the Timing Section by only storing samples when there is a change in data. No samples are stored if the data does not change. A transition in data occurs when at least one channel value changes from a logic high (1) to a logic low (0) or from a logic low to a logic high. When data is displayed, the timestamp is used to accurately reconstruct the data samples as they occurred.

Transitional acquisition mode becomes valuable when you need to monitor high-rate or widely-separated bursts of data. This is useful when testing disk drives, telecommunications devices, serial data or asynchronous buses, and electromechanical and process control applications where events happen slowly or infrequently.

If the data is changing frequently, a data sample is stored for each clock cycle, causing this mode to act like traditional asynchronous timing. In such cases, transitional acquisition will not extend memory. Memory fills rapidly even if only one channel is changing frequently.

Figure 3-9 shows the difference in the number of samples stored between an acquisition using the transitional acquisition mode and a traditional asynchronous acquisition.

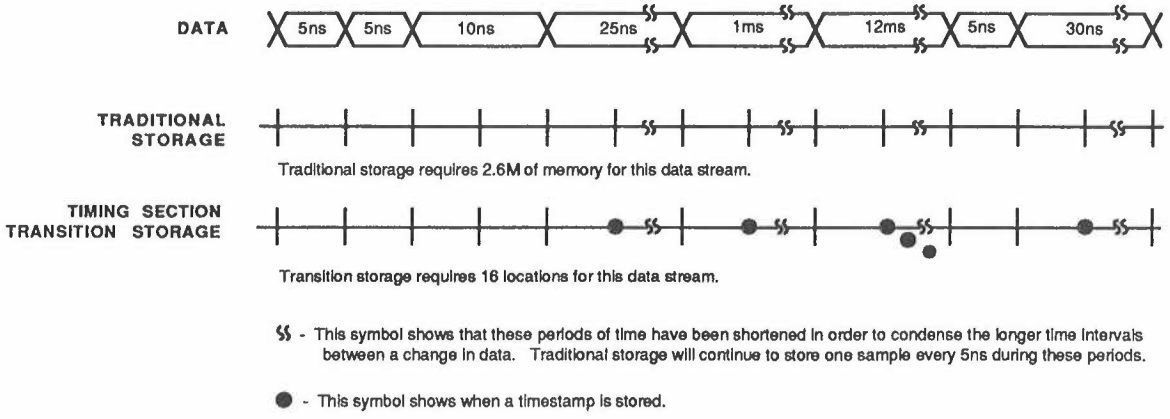


Figure 3-9. Transitional acquisition storage versus traditional asynchronous storage. The resolution of the data shown here is 5 ns. When data rates are 10 ns and faster, there is no difference between the two modes of storage. When the data rates are slower or come in bursts, the transitional mode is more efficient.

Synchronous Acquisition Mode

Use Synchronous Acquisition mode when you want data samples each time the SUT clock pulses.

In synchronous acquisition mode the Timing Section samples data based on the clock rate of the SUT (up to 90 MHz). You must connect channel 9 of the P6486 to the clock line of the SUT to sample data synchronously. You can choose to sample data on either the rising or falling edge of the SUT's clock.

To guarantee that synchronously acquired data is properly sampled, the data must be stable (valid) around the clock edge. The terms used for the required time that data must be valid are setup time and hold time.

Setup time. The amount of time a signal must be valid *before* the clock edge occurs in order to be recognized.

Hold time. The amount of time the signal must be valid *after* the clock edge occurs in order to be recognized.

The minimum setup time for the standard leadset is 2.5 ns before the clock edge; the minimum hold time is 1.0 ns after the clock edge. The minimum setup time for the high performance leadset is 1.5 ns before the clock edge; the minimum hold time is 1.0 ns after the clock edge. Figure 3-10 shows how data is sampled in synchronous mode and the minimum setup and hold time using the standard leadset.

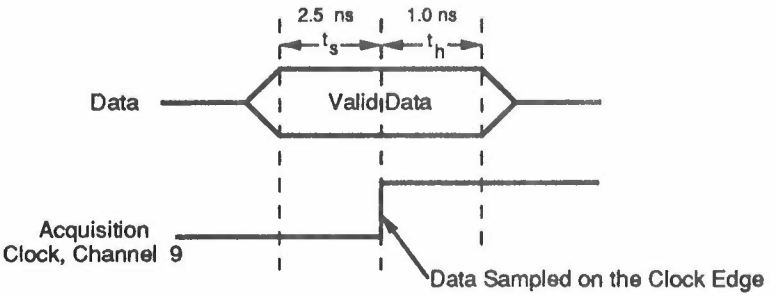


Figure 3-10. Minimum setup and hold times for synchronous mode using the standard leadset. The corresponding setup and hold time for the high performance leadset is 1.0 ns setup and 2.5 ns hold time.

To accurately compare a reference memory to an acquisition memory, both must be acquired using the synchronous acquisition mode. This is to ensure that you acquire each data sample at equal time increments (using the SUT clock). If you try to compare memories acquired using the transitional acquisition mode, no two acquisitions will be exactly alike due to the random nature of asynchronous sampling (compared to the SUT clock). Consequently, any comparison of the reference memory and acquisition memory will fail.

Timing Section Off

Selecting Off disables the Timing Section from participating in the system trigger. Selections concerning the Timing Section are removed from other menus such as the Execution Control, State Display, Timing Display, and display search menus.

Selecting the Trigger Position

The selected trigger position controls the amount of post-trigger acquisition memory. The amount of pre-trigger memory that is filled with data varies depending on how soon the trigger occurs after starting the acquisition. If the trigger event occurs immediately after the start of an acquisition, there may be no data before the trigger, regardless of the selected trigger position.

Choose the trigger location by placing the cursor on the Trigger Position field and pressing SELECT to cycle through the five trigger location choices.

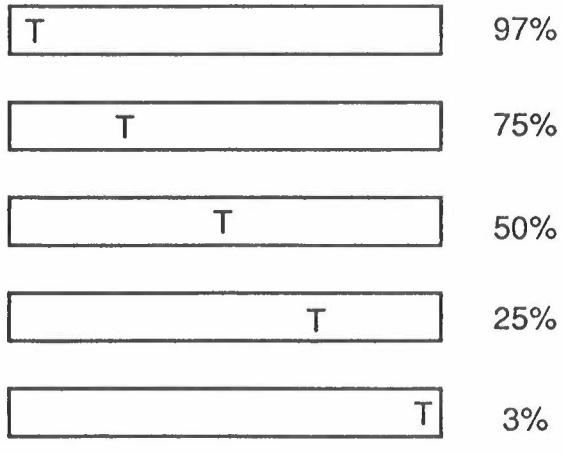


Figure 3-11. Trigger location.

Figure 3-11 shows the visual representation on the screen and the amount of post-fill (as a percentage of memory) represented by each trigger location choice. The rectangle represents the total memory available in the mainframe. The T represents the location of the trigger in relation to the total memory. Total memory available to store acquisitions in an MPM module is 8 Kilobytes.

Some examples of where to position the trigger are as follows:

- Position the trigger near the beginning of memory if you want to view the data samples occurring after the trigger event.
- Position the trigger near the end of memory if you want to view the data samples occurring prior to the trigger event.
- Position the trigger in the middle of memory if you want to view the data samples occurring both before and after the trigger event.

NOTE

If the trigger condition is met on the first sample acquired, the trigger will be displayed at the first location, regardless of which trigger location was selected because there will be no pre-fill data.

The acquisition does not end until post-fill is complete. If your trigger specification is such that the post-fill is never completed, the acquisition never ends. Press the Start/Stop key to recover.

Selecting the Acquisition Threshold Voltage

The acquisition threshold voltage is the voltage to which the input signals are compared. Signals below this voltage are logic low (0); signals above this voltage are logic high (1).

You can select the logic threshold voltage as either TTL, ECL, CMOS, or VAR. The variable (VAR) threshold allows you to enter a voltage value from +10 V to -10 V in increments of 50 mV using the standard leadset and from +5 V to -5 V in increments of 25 mV using the high performance leadset. The default variable threshold voltage is +1.4 V. The other acquisition threshold voltages are shown in Table 3-4.

Table 3-4
ACQUISITION THRESHOLD VOLTAGES

Selection	Voltage threshold
TTL	+1.4 V
ECL	-1.3 V
CMOS	±2.5 V*
*Assumes +5 V CMOS	

Creating a Trigger Specification

The trigger specification tells the Timing Section when to stop acquiring data, the event to recognize, and the action to take when the event occurs.

Trigger Arming. A condition that must be satisfied (usually a signal from another module) before the analyzer will begin to test the data.

Test. A condition that must be met before the analyzer will perform the stipulated action.

Action. Instructions that the analyzer must carry out when the trigger is found.

To set up a trigger specification, you must define the following:

- channel groups
- when to start the trigger search (arming)
- channel group values on which to trigger
- an action to perform

Defining Channel Groups

You must use the Channel Grouping submenu to specify the individual acquisition channels and organize them into logical groups. The groups are then available in a variety of menus for data entry and display. You can give each channel group a meaningful name and define the radix in which to display that group's data.

Channel. An input signal line which is assigned a number by which each signal from the probe is identified.

Group. An organization of a number of channels to form a meaningful combination, such as a 16-bit or 32-bit word.

You can change the default channel groups or create new ones. The default channel group setup is shown in Figure 3-12. You can use this default setup with either the standard or high performance leadsets when operating in either synchronous or transitional acquisition modes.

Press F6: Channel Grouping to access the Channel Grouping submenu. Use function keys F1: Add Next Channel, F2: Insert Channel, and F5: Delete Channel to add and delete channels to and from any group. Use function keys F3: Add Group and F6: Delete Group to add and delete channel groups. You can assign the same channel to more than one group.

Figure 3-12 shows the Channel Grouping submenu.

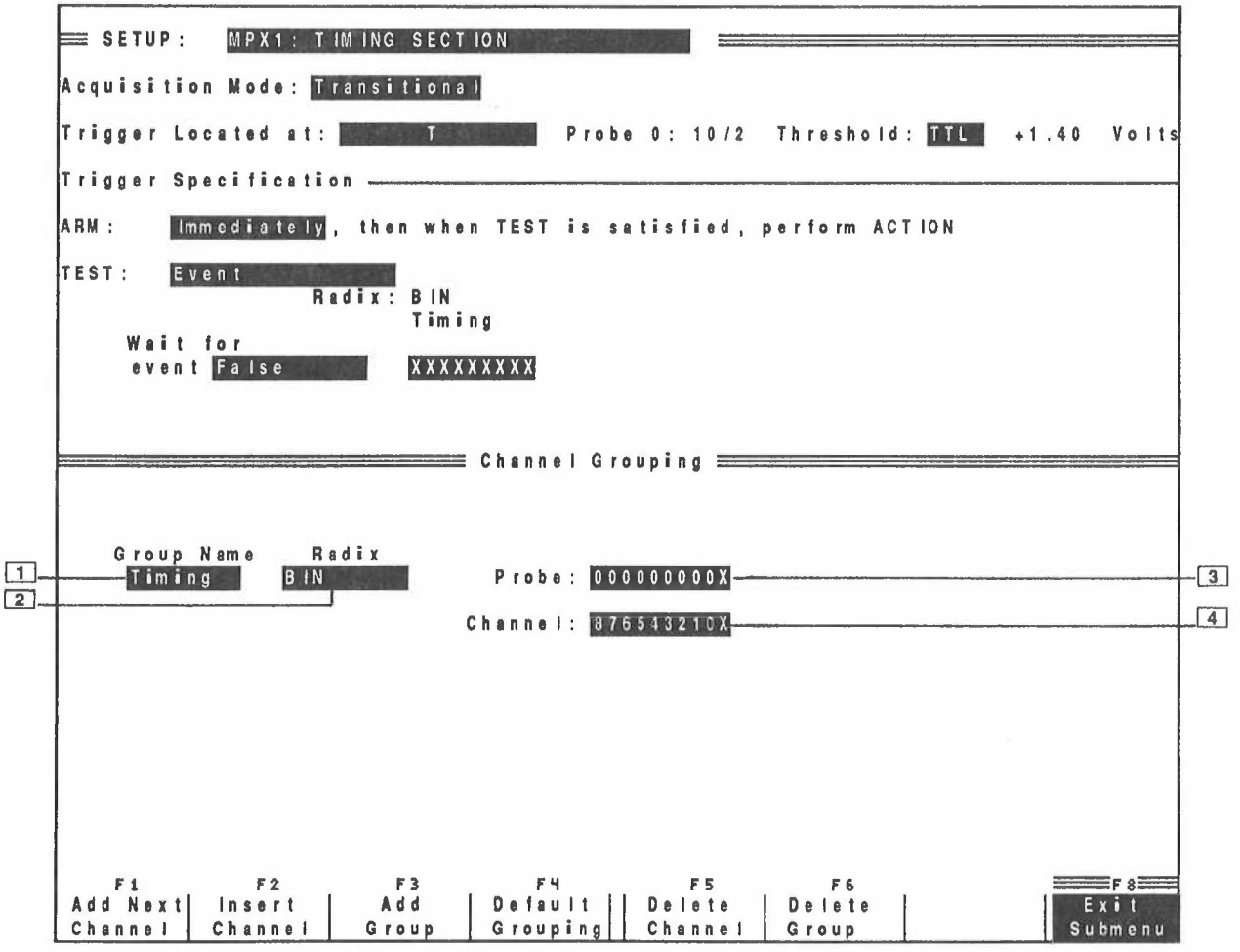


Figure 3-12. Channel Grouping submenu showing the default setup.

1 **Group Name.** Lets you name each channel group. You can use up to eight alphanumeric characters in a name and can define up to 10 groups.

2 **Radix.** Lets you choose an input radix for the channel group. Selections are BINary, OCTal, HEXadecimal, and SYMBOL.

3 **Probe.** Shows the number of the P6486 probe that is connected to the Timing Section.

4 **Channel.** Lets you select which probe channels to include in the group. The channels are the same for both the standard and high performance leadsets. You can assign the same channel to more than one group.

Function Keys

F1: Add Next Channel. Adds the next lower-numbered channel to the right of the cursor. You can only add the next channel when the cursor is in a Probe or Channel field.

F2: Insert Channel. Adds an undefined channel (an X) to the left of the cursor. You can only insert a channel when the cursor is in a Probe or Channel field.

F3: Add Group. Adds a new channel group below the group the cursor is positioned on.

F4: Default Grouping. Replaces the current channel group setup with the default channel group setup as shown in this figure. A prompt will ask you to confirm this change.

F5: Delete Channel. Deletes the channel the cursor is positioned on.

F6: Delete Group. Deletes the channel group the cursor is positioned on .

F8: Exit Submenu. Leaves the Channel Grouping submenu and returns to the Timing Section setup menu. The Timing Section setup menu will reflect the new channel groups.

Each channel group has a group name field, a radix field, a probe field, and a channel field. The following paragraphs explain how to use these fields to create a channel group.

The maximum number of channel groups allowed is 10.

Entering a Channel Group Name. You can enter up to eight alphanumeric characters in the channel group name field. The maximum number of channel groups allowed is 10. If you want to change a group name, you must change it in the Channel Group submenu.

The channel groups are displayed in these various menus in the same order as they appear in the Channel Grouping submenu. Every menu, except Timing Display, shows the channel groups horizontally in descending-bit order from left to right. The Timing Display shows the channel groups vertically in descending-bit.

Selecting a Radix. You can select the input radix for the channel group values in the Channel Grouping submenu. The choices are binary (BIN), octal (OCT), hexadecimal (HEX), and symbol (SYMBOL).

Use F5 to change the radix.

You can also change the radix of the channel group that the cursor is positioned on using the Timing Section Setup menu by pressing F5: Change Radix. Pressing F5 cycles through the radix choices and changes the width of the channel group accordingly.

A symbol table is a file of alphanumeric symbolic names associated with data values. If you select symbol as the radix, the symbol that corresponds to a channel group value is used in place of the actual group value. If there is no symbol table available, or the channel group value has no symbol defined for it, then the label UNDEFINED appears for that channel group or channel group value.

Symbols are mnemonics that you create to help you easily identify numeric values. You can use the symbol radix if you have already created a symbol table in the Symbol Definition Edit menu or if you have downloaded a symbol table from a host computer or other software application (such as microprocessor support).

The analyzer uses the symbol table to translate numbers to alphanumeric mnemonics. In other words, the program goes to the table, looks up a numeric value, and substitutes the symbol entry for that number (or UNDEFINED if no symbol exists). The symbol is then displayed in the State Table Display menu where the alphanumeric value would be. You can also use the symbol as the word recognizer in the trigger specification portion of the Timing Section setup menu.

As an example of using symbols, suppose that an interrupt subroutine starts at address FC. You can define a symbol corresponding to that value such as "intsub1". You can then enter "intsub1" in the word recognizer field of the Trigger Specification portion of the Timing Section Setup menu, thereby causing the Timing Section to trigger when "intsub1" (actually FC) occurs on the address bus. If you specify symbolic radixes for the State Table Display menu, the symbol "intsub1" will appear for every data sample in the address group with a value of FC.

For a complete description of symbols, refer to the section *Using Symbols* in the mainframe user's manual

Arming

When you arm a module or section, you are defining a pre-condition that must be met before performing the trigger test.

If you choose to trigger on an Event, the arming choices are Immediately, On Signal 1, On Signal 2, On Signal 3, or On Signal 4. The signal must be set by another module or module section before the Timing Section can look for the trigger event word recognizer. Choosing Immediate allows the Timing Section to immediately start looking for the trigger event without waiting for a signal.

If you choose to trigger on an Event and Signal, then the Timing Section arms immediately after you press Start, Auto, or Cont.

Selecting a Trigger Test

Use the Test field to specify the type of trigger test for the Timing Section to perform. You can choose either Event or Event and Signal.

When you choose to trigger on an event, you must enter a word recognizer value for the channel groups. After starting an acquisition, the probe connecting the Timing Section to the SUT begins looking at data from the channels to which it is connected. A data sample is acquired and stored each time either a synchronous-active-clock edge occurs in Synchronous mode or there is a change in data in Transitional mode. Each data sample is compared to the trigger event word to see if that sample matches the trigger event. When a match is found, the analyzer continues to fill acquisition memory as defined by the trigger position field, the logic analyzer sets an optional signal, and data is displayed.

When you choose to trigger on an event and signal, a signal must also be set from another module or section when the Timing Section trigger event word is located for the selected action to be performed. (In transition mode, the signal may be set prior to locating the trigger event word or vice versa. In synchronous mode, the signal must be set before or coincident with the active clock edge.)

Changing the Channel Group Radix

The Channel Group Radix field shows the input radix that is defined in the Channel Grouping submenu. To change the radix in the Timing Section Setup menu, position the cursor on the word recognizer field and press F5: Change Radix until you select the desired radix (Binary, Octal, Hexadecimal, or Symbol).

Choosing to Trigger on a True or False Event

The Trigger Event True/False field lets you set up the Timing Section to look for the value as entered in the trigger event word recognizer field (True) or to look for any value different (False).

Defining the Trigger Event Word Recognizer

The Trigger Event Word Recognizer field lets you enter a value for each channel group. The Timing Section compares each data sample against these channel group values. The results are then used to determine if the trigger event is satisfied.

You may enter any value according to the channel group input radix (binary, octal, hexadecimal, or symbol). You can also use function key F1: Load From Cursor to load the channel group value from the active data cursor in a display menu to the trigger event word recognizer field. Enter an X for any channel whose value you do not want to compare against.

Choosing the Action to Perform

You can set up the logic analyzer to take a number of different actions after it finds the trigger event: Trigger Section, Trigger System, Trigger Section and Set Signal (1-4), and Trigger System and Set Signal (1-4).

Triggering the section causes the Timing Section's post-trigger circuitry to fill the specified amount of memory and stop. The acquired data is then displayed.

Triggering the system causes the Timing Section to trigger all the other modules or sections that haven't already triggered. Again, the post-trigger circuitry fills the specified amount of memory, stops, and displays data. Triggering the system also drives the Trigger Out signal (a BNC connector on the mainframe's rear panel). Refer to the mainframe user's manual for a description of the Trigger Out signal.

Triggering the system and setting a signal, and triggering the section and setting a signal act as previously described with one additional action, a signal (1-4) is set. Other modules or sections can use this signal for arming or as part of their trigger test event. You cannot set a signal already being used for arming or testing.

DISPLAYING TIMING DATA

The Timing Diagram Display is a graphic view of the changing values for each channel shown as a digital waveform. You can also view Timing Section data in the State Table Display format. Figures 3-3 through 3-7 show examples of the Timing Diagram Display format. Refer to your mainframe user's manual for an in-depth description of the Timing Diagram Display format.

Acquisition Status Screen

The Acquisition Status screen appears immediately after an acquisition begins. The status information can help you spot a problem in your setup, such as a trigger test specification that causes the analyzer to never find the trigger event.

If the trigger event is not found, then you should check the following:

- connections to the SUT
- channel grouping
- trigger event word recognizer value
- threshold voltage
- arming on a signal

When the acquisition is 100% complete, the data samples are displayed. For more information about the acquisition status display, refer to the section *Acquiring Data* in the system user's manual.

Timestamp Values and Shared Memory

Timestamp values show how much time has elapsed between data samples. They are also used to time-correlate data from other modules and sections with Timing Section data.

Timestamp values and data samples share the same memory. As data sampling rates become slower, more of the memory is used to store timestamp values. This means that there are fewer data samples in memory. Refer to Figure 3-13 to view a graph showing the data rate versus the number of data samples stored in memory.

The data sampling rate in transitional acquisition mode can be as fast as 200 MHz yielding 2 kilobytes of data samples; the data sampling rate in synchronous acquisition mode can be as fast as 90 MHz yielding 1 kilobyte of data samples.

You can view the timestamp value in the State Display menu as time from previous sample (relative) or time from sample trigger (absolute). Refer to the State Display section of this manual for a description of displayed timestamp values.

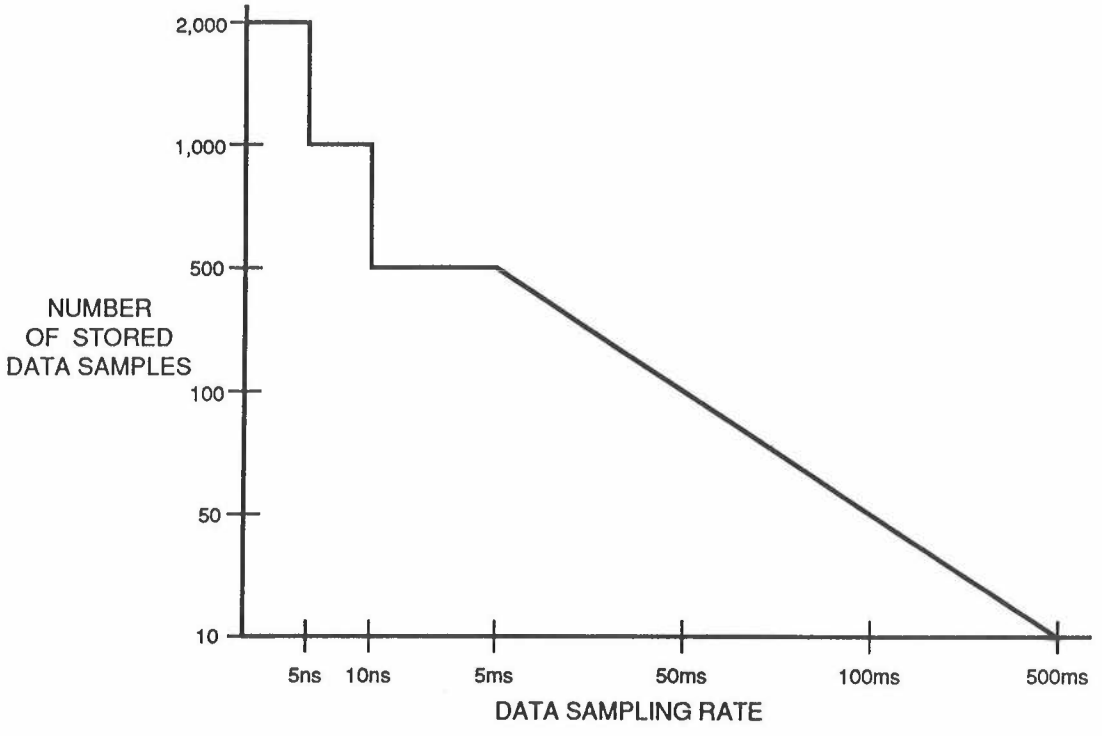


Figure 3-13. Data rate versus number of data samples stored in memory. This graph shows the maximum number of data samples stored in memory for various sampling rates.

Table 3-5 shows the size of the time window in which data can be acquired by the Timing Section at various data rates. This can help you determine how to specify the trigger test.

Table 3-5
ACQUISTION WINDOW SIZE

Data Rate	Minimum Time	Maximum Time
5 ns -10 ns	10.2 us	10.2 us
10 ns -5 ms	10.2 us	2.68 s
5 ms -50 ms	2.68 s	4.39 s
50 ms -100 ms	4.39 s	5.08 s
100 ms -500 ms	5.08 s	5.19 s

SAVING TIMING SECTION SETUPS

Once you define a Timing Section setup, you can save it on either floppy disk or hard disk using the Save Module Setup command in the SAVE/RESTORE Utility menu. Once you have saved the setup, you can restore it for use in other logic analyzer sessions. For instructions on using the Save Module Setup and Restore Module Setup commands refer to the section *Using Utilities* in the system user's manual.

SAVING TIMING SECTION DATA

You can save the current Timing Section acquisition memory as a reference memory. The memory can be saved on either floppy disk or hard disk using the Save Acqmem and Save Refmem commands in the SAVE/RESTORE Utility menu. Once you have saved them, you may use acquisitions by using the Restore Refmem command in the SAVE/RESTORE Utility menu. For instructions on using the Save Acqmem, Save Refmem, and Restore Refmem commands refer to the section *Using Utilities* in the system user's manual.

Section 4: USING MNEMONIC DISASSEMBLY

The MPM module supports mnemonic disassembly and analysis for a variety of popular microprocessors. This support consists of a probe adapter, which has been configured for the particular microprocessor you are disassembling, software to disassemble the signals from the microprocessor, and a manual with information that is specific to the microprocessor your disassembler supports.

Probe. The hardware which connects the mainframe to a probe adapter, usually composed of a connector to the mainframe, a cable, a plastic housing containing a circuit board, and a connector to the probe adapter.

Probe Adapter. The hardware which connects the probe to the SUT, usually composed of a connector to the probe, a plastic housing containing a circuit board, one or more cables, and a microprocessor socket that plugs into the SUT.

How to Use This Section

This section contains the information common to all microprocessors which are supported. You will find more specific information about the particular disassembler you are using, such as pinout tables, channel menu setups, cycle types, etc., in the user's manual that came with your disassembler.

Disassembler Components

Your mnemonic disassembly package consists of these items:

- **Probe Adapter.** You will receive a probe adapter with your mnemonic disassembly package. This probe adapter has a plastic shell and a 120-pin connecter that plugs into the P6480 on one end, and a target head that connects to your SUT on the other end. More information about connecting the probe adapter follows later in this section.
- **Probe Latches.** You will find two plastic probe latches. These are used to secure the probe adapter to the P6480 probe. For more information on using the probe latches, see the section *Making Connections*, later in this manual.
- **Software Disk.** You will find files on your software disk. For the names of the files, refer to the user's manual that came with your disassembler.

- **Manual.** You will receive a manual that has information specific to the microprocessor supported by the disassembler package. This section frequently referrs to this manual.

GETTING STARTED WITH MNEMONIC DISASSEMBLY

Using the FasTrak board, you can quickly take a data acquisition that will show you many of the features of mnemonic disassembly.

1. Make sure the PRISM and the FasTrak are off.
2. Plug the P6480 into the PRISM.
3. Plug the P6480 into the connector labeled J100 on the FasTrak.
4. Power up the PRISM.
5. Power up the FasTrak.
6. Press and hold the reset button on the FasTrak while you perform the next step.
7. Press Start/Stop on the PRISM.
8. Release the reset button on the FasTrak.
9. When the acquisition has been taken, the State Table will be displayed.
10. Move the cursor down to the Data Format field and cycle through to Hardware or Software to see disassembled data.

INSTALLING THE DISASSEMBLER

In order to use the disassembler you must install the software and then make the proper connections between the SUT, leadset, probe and mainframe.

Installing the Software in the Mainframe

Installation of the software in the mainframe consists of copying the files from the disassembler disk to the hard disk in the mainframe or to a floppy disk that has been configured as an applications disk.

Hard Disk Installation

To install the disassembler software on a hard disk, perform the following steps:

1. Power up the mainframe.

2. Insert the mnemonic disassembly software disk in the floppy drive of the mainframe.
3. Use the Copy File command to copy the files on the disk to the Support directory in the system. For instructions on how to use the Copy File command, refer to the section *Using Utilities* in the PRISM system user's manual.

For the exact names of the files which you must copy, refer to your specific mnemonic disassembly manual.

After performing this procedure, the disassembler will be loaded automatically when you power up the mainframe if the corresponding disassembler probe adapter is plugged into the P6480 state probe, and the P6480 is plugged into the mainframe.

Floppy Disk Installation

1. Power up the mainframe.
2. Install the system on a floppy disk. When you have finished you will have a system disk and an application disk. For instructions on installing the system on a disk, refer to the section *Using Utilities* in the PRISM system user's manual.
3. Create a subdirectory called Support on the application disk which you have just created. For instructions on creating a subdirectory, refer to the section *Using Utilities* in the PRISM system user's manual.
4. Using the Copy File command, copy the files from the mnemonic disassembly software disk to the support directory on the application disk. For instructions on how to use the Copy File command, refer to section *Using Utilities* in the PRISM system user's manual.

After performing this procedure, the disassembler will be loaded automatically when you boot from the floppy disk if the corresponding disassembler probe adapter is plugged into the P6480 state probe and the P6480 is plugged into the mainframe.

Making Connections

Connecting the disassembly probe adapter to the mainframe consists of three steps. Be sure the power to the PRISM and the power to the SUT is off before performing the following steps:

1. Connect the P6480 probe to the mainframe.
2. Connect the disassembler probe adapter to the P6480.

3. Connect the disassembler probe adapter target head to the SUT.

CAUTION

To avoid damage to the system or to the SUT, be sure the power to both systems is off before making any probe or leadset connections.

Connecting the P6480 Probe to the Mainframe

To connect the P6480 State Probe to the mainframe, insert the P6480 State Probe cable connector into the State Section slot on the mainframe. The State Section slot is the one closest to the rear of the mainframe. This slot is keyed so that only the State Probe cable connector will fit in it and the State Probe cable connector will only fit one way.

Press the button labeled ID on the probe for probe and leadset information.

To identify which State Section the state probe is connected to, press the button labeled "ID" on the P6480. The module or section number to which the timing probe is connected will be displayed on the top line of the screen. An example of such an ID number is "MPM1: Internal Probe 1 with No Leadset."

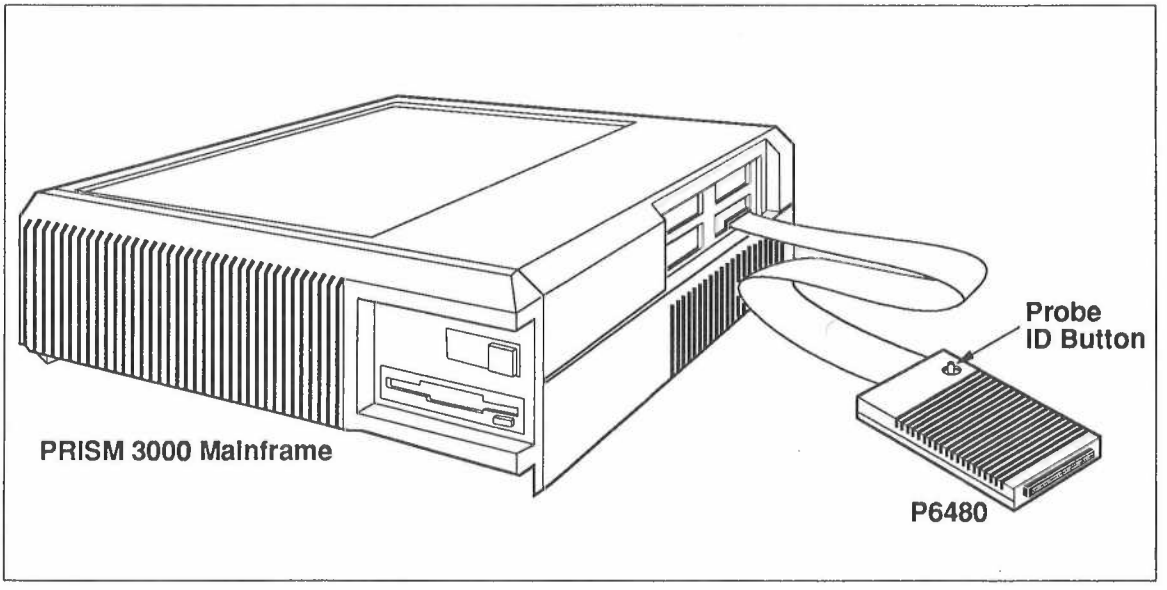


Figure 4-1. P6480 probe connected to the mainframe.

Connecting the Disassembler Probe Adapter to the P6480

To connect the probe adapter to the P6480 State Probe perform the following steps:

1. Align the connector of the disassembler probe adapter (label side up) with the connector of the P6480 (label side up).
2. Plug the disassembler probe adapter into the P6480. The connectors on both the probe adapter and the P6480 are keyed, so you cannot plug them in wrong.
3. Insert the probe latches by pushing the points of the latches into the loops of the probe and probe adapter.

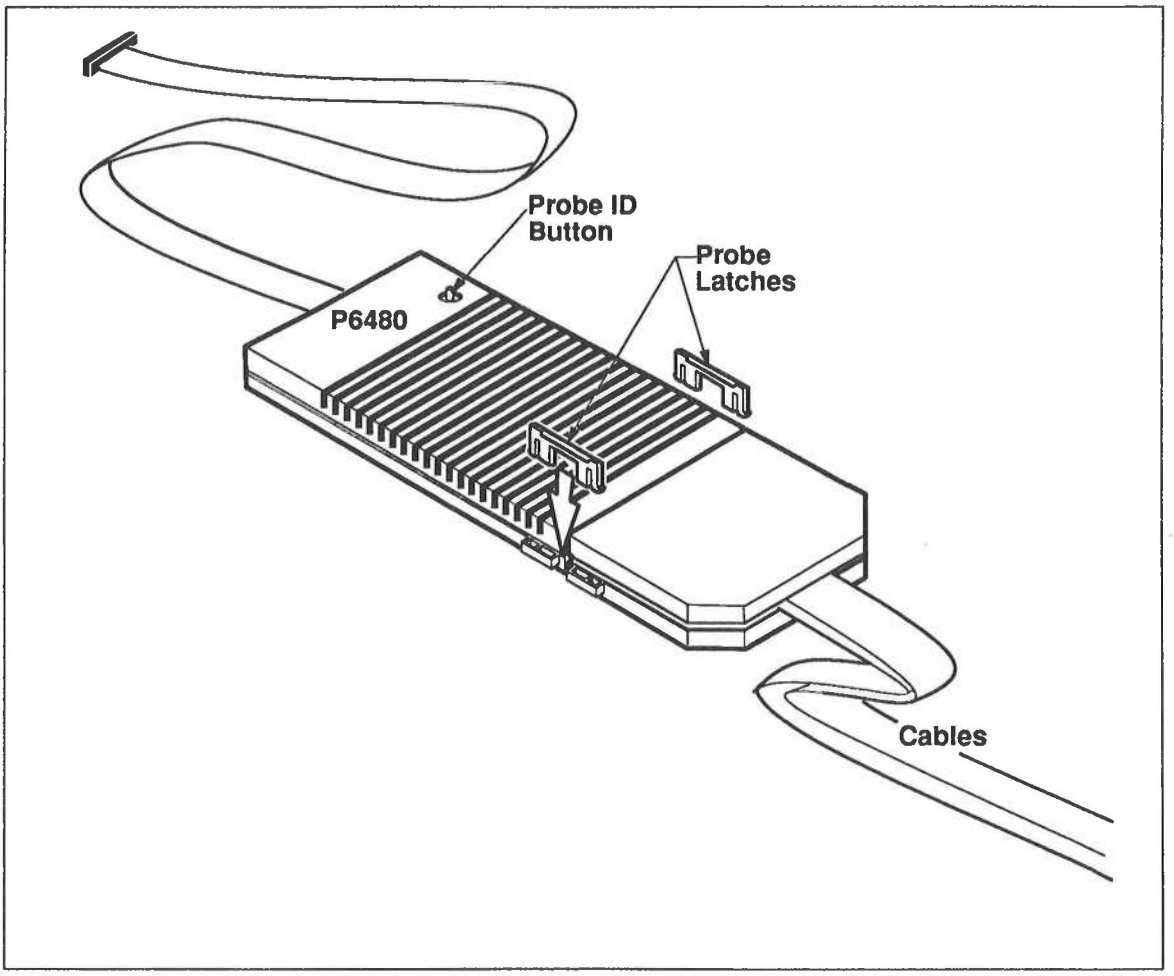


Figure 4-2. Disassembly probe adapter connected to P6480.

Connecting the Disassembler Probe Adapter to the SUT

Connecting the probe to the SUT depends on the disassembler you are using and the package style of the microprocessor in the SUT. Refer to the table *Chip Packages Supported* in your specific mnemonic disassembly manual to see which procedure to follow to connect to the SUT.

Socketed DIP (Dual In-Line Package)

If the microprocessor in the SUT is in a DIP package that is socketed onto the SUT board, refer to Figure 4-3 and perform the steps that follow to connect the disassembly probe adapter to the SUT.

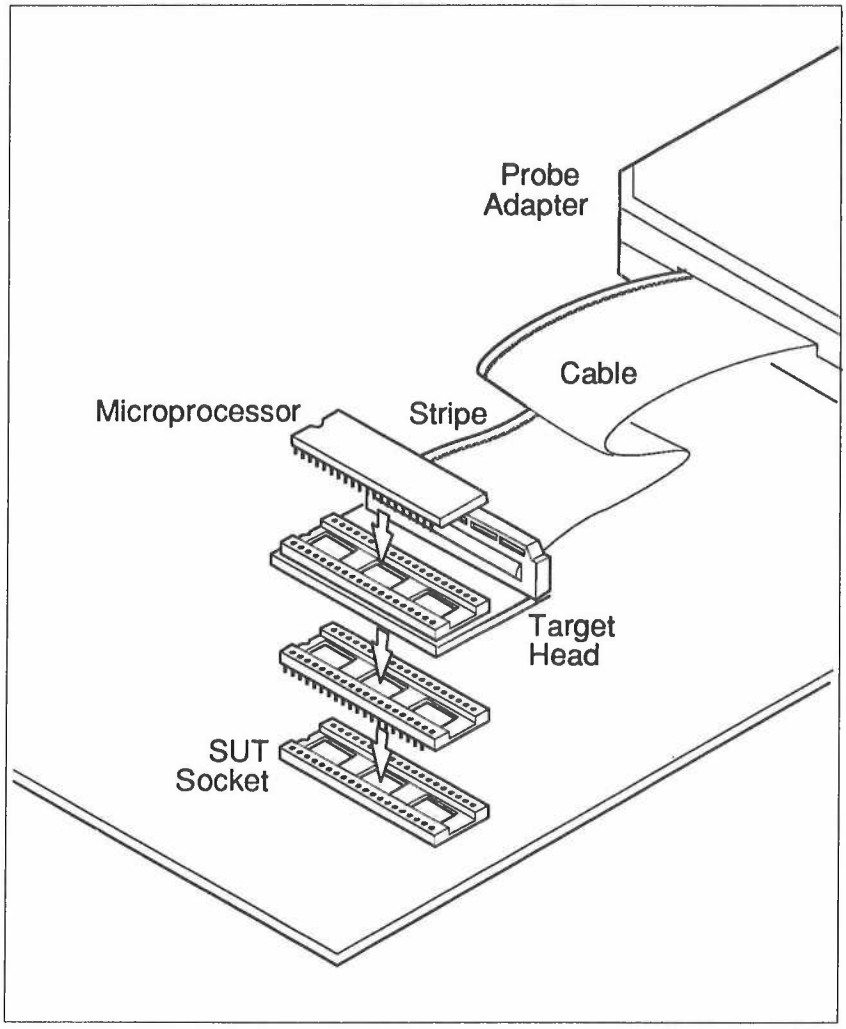


Figure 4-3. Connecting the disassembly probe adapter to a socketed DIP.

1. Make sure the power is off to both the mainframe and the SUT.
2. Remove the microprocessor from the SUT.

CAUTION

To avoid damage to the microprocessor, observe standard static precautions when handling the microprocessor.

3. Lining up the notch on the target head socket with the notch on the SUT microprocessor socket, insert the socket of the disassembly probe adapter target head in the SUT microprocessor socket.
4. Lining up the notch of the microprocessor with the notch of the target head socket, insert the SUT microprocessor in the disassembly probe adapter target head socket.
5. Power up the PRISM.

CAUTION

To avoid damage to the analyzer or to the system under test, always power up the analyzer before powering up the SUT.

6. Power up the SUT.

Soldered DIP (Dual-In-Line Package)

If the microprocessor in the SUT is in a DIP package that is soldered onto the SUT board, refer to Figure 4-4 and perform the steps that follow to connect the disassembly probe adapter to the SUT.

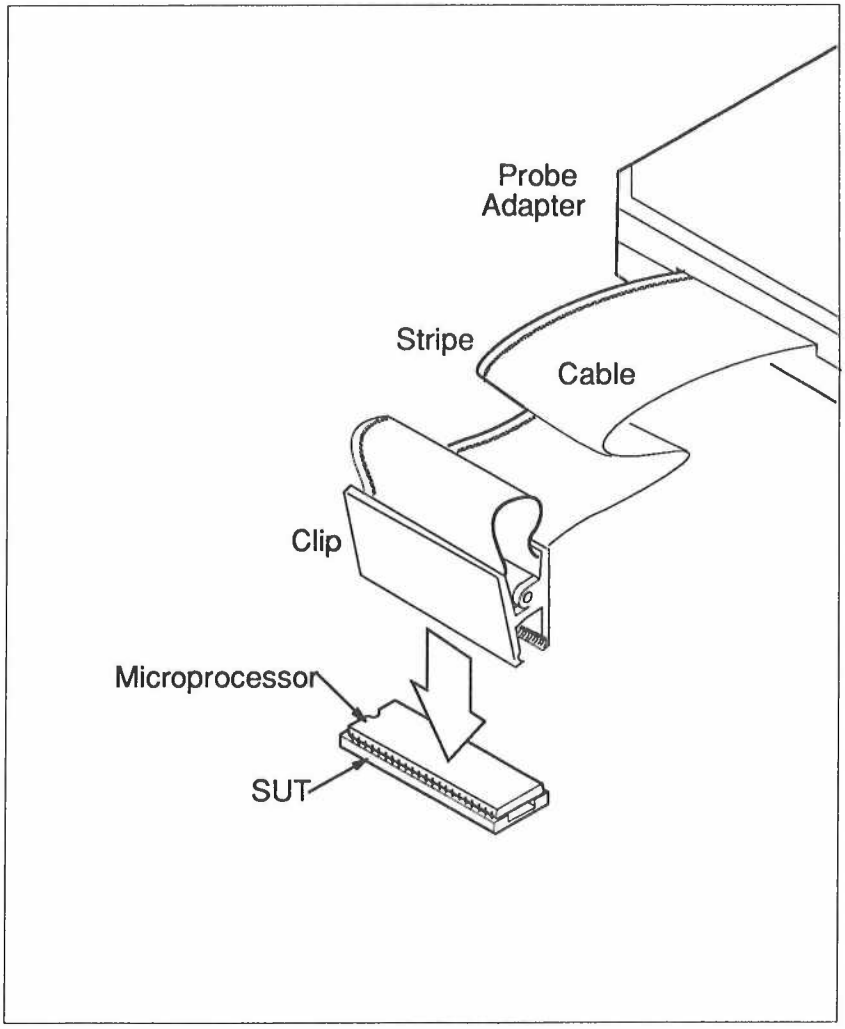


Figure 4-4. Connecting the disassembly probe adapter to a soldered DIP.

1. Make sure the power is off to both the mainframe and the SUT.

2. Line up the stripe of the cable of the DIP clip with pin 1 on the SUT microprocessor socket. Clip the DIP clip of the disassembly probe adapter on the SUT microprocessor.

CAUTION

To avoid damage to the microprocessor, observe standard static precautions when working near the microprocessor.

3. Power up the PRISM.

CAUTION

To avoid damage to the analyzer or to the system under test, always power up the analyzer before powering up the SUT.

4. Power up the SUT.

Socketed PGA (Pin Grid Array)

If the microprocessor in the SUT is in a PGA package, refer to Figure 4-5 and perform the steps that follow to connect the disassembly probe adapter to the SUT.

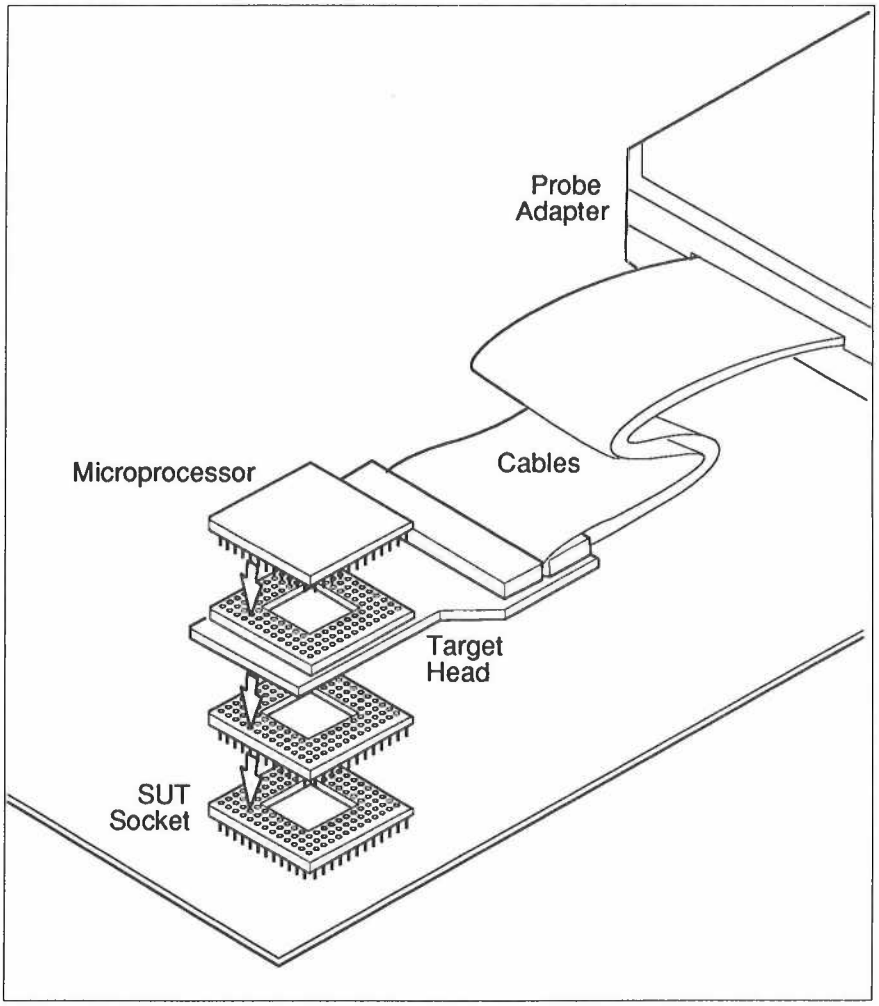


Figure 4-5. Connecting the disassembly probe adapter to a socketed PGA.

1. Make sure the power is off to both the mainframe and the SUT.

2. Remove the microprocessor from the SUT.

CAUTION

To avoid damage to the microprocessor, observe standard static precautions when handling the microprocessor.

3. Line up the pin 1 indicator on the target head circuit board with the pin 1 indicator on the SUT microprocessor socket and insert the socket of the disassembly probe adapter target head in the SUT microprocessor socket.

NOTE

If Pin 1 is not designated, the PGA socket is keyed; there is only one way the PGA will fit in the socket.

4. Line up the pin 1 indicator of the microprocessor with the pin 1 indicator of the target head circuit board and insert the SUT microprocessor in the disassembly probe adapter target head socket.
5. Power up the PRISM.

CAUTION

To avoid damage to the analyzer or to the system under test, always power up the analyzer before powering up the SUT.

6. Power up the SUT.

Socketed PLCC (Plastic Leaded Chip Carrier)

If the microprocessor in the SUT is in a PLCC package that is socketed onto the SUT board, you will receive a PGA probe adapter and two PGA-PLCC converters. The PGA-PLCC converters should come already attached to the PGA probe adapter. If the converters should become separated from the probe adapter, note that the converter consisting of a PLCC socket and PGA pins goes on the top side of the target board and the converter consisting of a PGA socket and PLCC pins goes on the under side of the target board.

Refer to Figure 4-6 and perform the steps that follow to connect the disassembly probe adapter to the SUT.

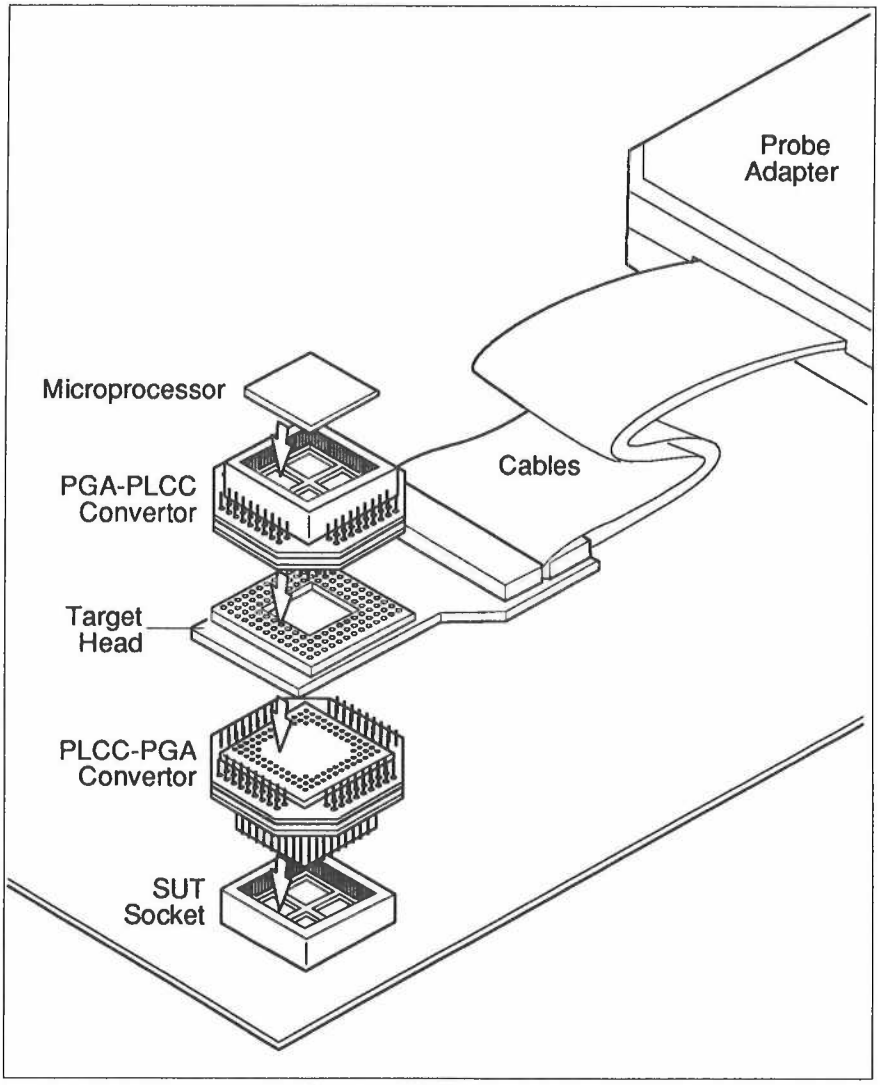


Figure 4-6. Connecting the disassembly probe adapter to a socketed PLCC.

1. Make sure the power is off to both the mainframe and the SUT.
2. Be sure the PGA-PLCC converters are properly connected to the PGA disassembly probe adapter.

3. Remove the microprocessor from the SUT.

CAUTION

To avoid damage to the microprocessor, observe standard static precautions when handling the microprocessor.

4. Line up the pin 1 indicator on the PGA target head with the pin 1 indicator on the SUT microprocessor socket and insert the PLCC socket of the disassembly probe adapter target head in the SUT microprocessor socket.
5. Line up the pin 1 indicator of the microprocessor with the pin 1 indicator of the PGA target head socket and insert the SUT microprocessor in the PLCC disassembly probe adapter target head socket.
6. Power up the PRISM.

CAUTION

To avoid damage to the analyzer or to the system under test, always power up the analyzer before powering up the SUT.

7. Power up the SUT.

Soldered PLCC (Plastic Leaded Chip Carrier)

If the microprocessor in the SUT is in a PLCC package that is soldered onto the SUT board, you will receive a quad clip and a flying leadset instead of a disassembly probe adapter. The quad clip attaches to the microprocessor, and the flying leadset barrel connector lead tips attach to the pins on the quad clip. For information regarding making pin connections, refer to the tables *Control Group Channel Assignments*, *Address Group Channel Assignments*, and *Data Group Channel Assignments* in your mnemonic disassembly manual. Refer to Figure 4-7 and perform the steps that follow to connect the disassembly probe adapter to the SUT.

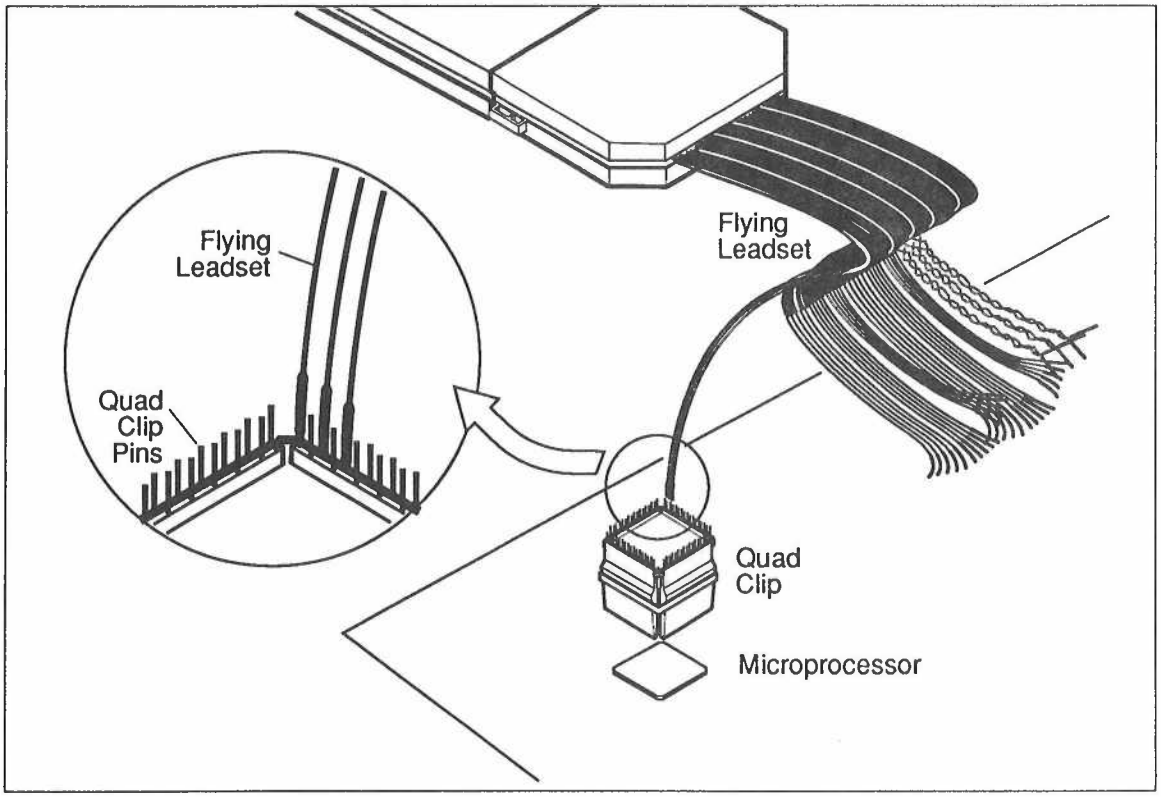


Figure 4-7. Connecting the disassembly probe adapter to a soldered PLCC.

1. Make sure the power is off to both the mainframe and the SUT.
2. Pull the handles of the quad clip up.

3. Push the quad clip on the microprocessor.

CAUTION

To avoid damage to the microprocessor, observe standard static precautions when working near the microprocessor.

4. Slide the handles of the quad clip down to secure the quad clip on the microprocessor.
5. Attach the GPPA leads to the appropriate pins of the quad clip.
6. Power up the PRISM.

CAUTION

To avoid damage to the analyzer or to the system under test, always power up the analyzer before powering up the SUT.

7. Power up the SUT.

Loading the Software

You can load the mnemonic disassembly software manually, or you can allow the system to load the mnemonic disassembly software automatically. If you have installed the mnemonic disassembly software on the hard drive in the mainframe, you can allow the system to load the software automatically.

If you have a disassembler probe connected to the mainframe when you power up, the disassembler will automatically be loaded. If you are booting from a floppy disk, the mnemonic disassembly software must be in the support directory on the application disk. The disassembler will not automatically load if the microprocessor is in a soldered PLCC package.

NOTE

You can load only one disassembler to an MPM module. If you need more than one disassembler, you must have more than one MPM modules.

You need to load the software manually if you change leadsets without turning the power off, then on again. To manually load the software use the Load Application command in the Utility: Save/Restore menu. If you have a hard disk, you will find the mnemonic disassembly software in the support directory. If you load from a floppy, you will find the mnemonic disassembly software in the support directory of your mnemonic disassembly disk. Refer to the mnemonic disassembly manual for the name of the file you must load.

ACQUIRING DATA WITH A DISASSEMBLER

The following steps are necessary to set up the system to make an acquisition:

1. Choose the clocking mode
2. Group the channels
3. Define symbols for the logic analyzer to recognize
4. Specify the trigger

Some of these steps are done for you by the disassembler. You can look at how the disassembler has set up the logic analyzer to acquire data. When there are choices for you to make in a particular field, those choices depend on which microprocessor disassembler is loaded.

For more information on setting up an acquisition, refer to *Using the State Section* in this manual.

Use F6 to access the Channel Grouping submenu or the Clocking Definition submenu.

Figure 4-8 shows the State Section in the Setup menu. In this menu, you can access Acquisition Mode and Clocking and Grouping menus. You can access the Clocking and Grouping menus by pressing F6: Clocking/Grouping. After you press F6, you will see either Group Definition or Clock Definition. Place the cursor on the word GROUP and press the SELECT key to toggle between Clock Definition and Group Definition.

Use Acquisition Mode by placing the cursor on the field and pressing the Select key to cycle through the choices. One choice that is always available to you is Off. This turns the state section off. If there are multiple disassemblers loaded at the same time, you can select the MPM module (and therefore which disassembler) will be affected by your following selections.

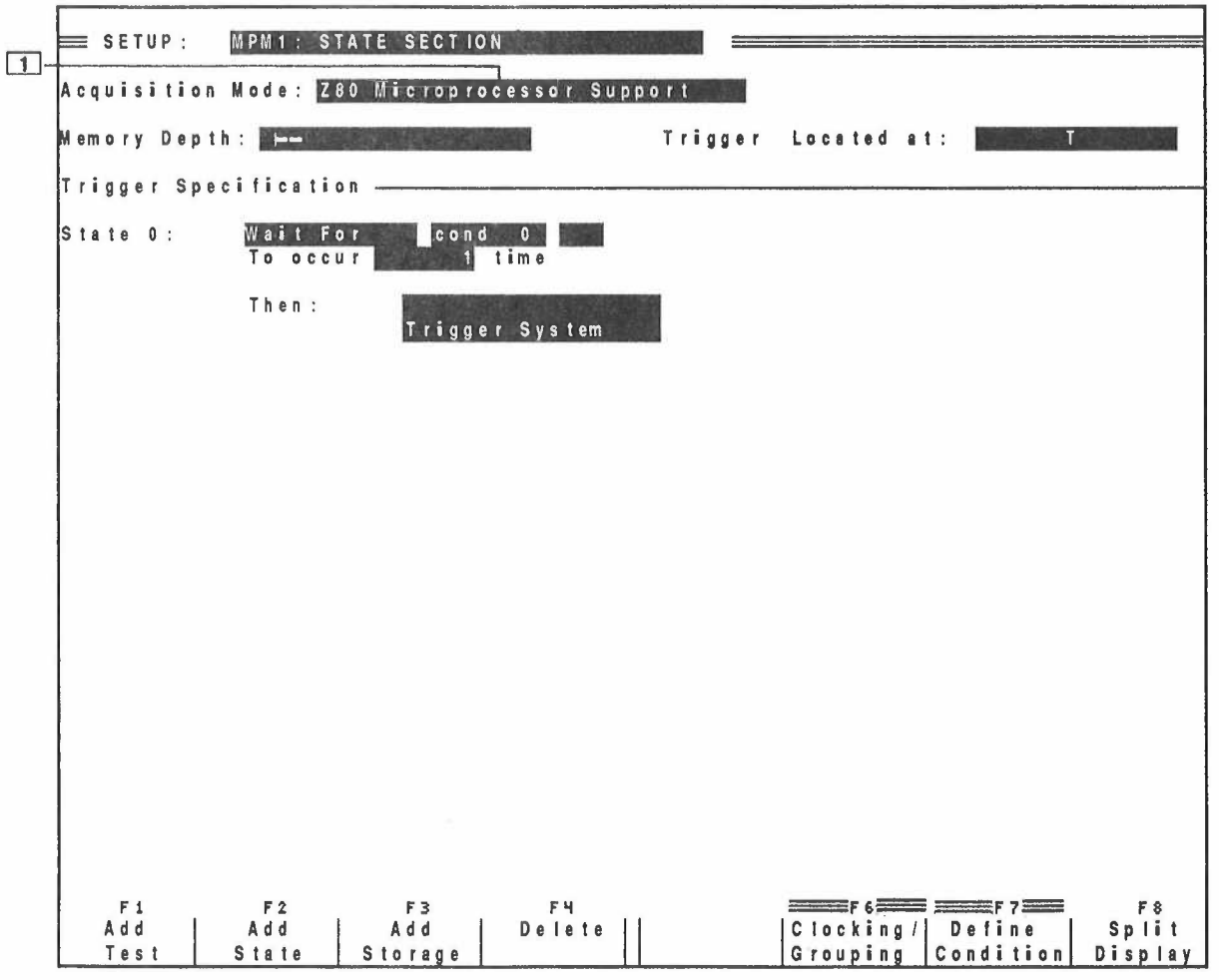


Figure 4-8. State Section Setup menu.

1 **Acquisition mode.** Press select to choose Off or the microprocessor being supported.

Function keys

F6: Clocking/Grouping. Press F6 to view Clocking and Grouping definitions.

Selecting the Clocking Mode

Selecting the clocking mode allows you to specify the cycle types you want the analyzer to recognize in addition to regular microprocessor bus cycles in your acquisition. The choices in the clocking type field depend on which microprocessor disasembler you are using. Figure 4-9 shows the Clocking Definition submenu. Refer to the your microprocessor disassembler manual to see the clocking mode choices available for the disassembler you are using.

When a clocking mode includes DMA cycles, these cycles can only be acquired if the DMA activity is visible on the microprocessor pins.

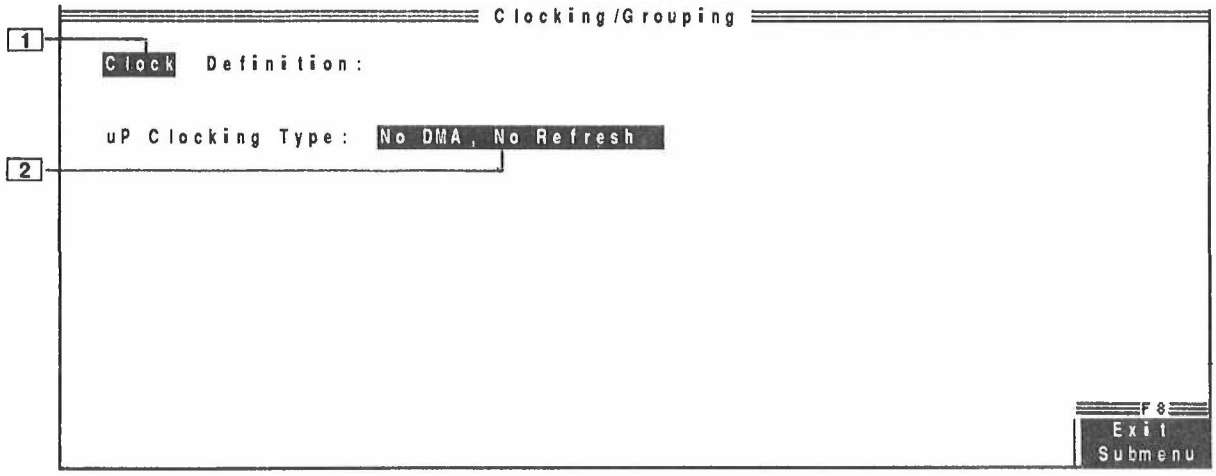


Figure 4-9. Clocking Definition submenu.

[1] **Clock.** Defines the acquisition clock.

[2] **Clocking Type.** This field shows the clocking modes you can use.

Function keys

F8: Exit submenu. Allows you to leave the Clocking Definition submenu.

To select the clocking mode, perform the following steps:

1. Display the State Setup menu by pressing the SETUP key and choosing STATE SECTION.
2. Display the Clocking/Grouping submenu by pressing F6 (Clocking/Channel definition).
3. In the Clocking/Grouping submenu, move the cursor to the Group or Clock Definition field. Press the SELECT key to toggle between Clock and Group definition. Choose Clock.
4. Place the cursor on the μP Clocking Type field and press SELECT to toggle through the choices. Select the choice you want.
5. Press F8: Exit Submenu.

Viewing the Channel Groupings

When you are using a microprocessor disassembler you cannot change the channel groupings. To see the channel groupings for the specific disassembler you are using you can refer to your disassembler manual, or you can look at the Channel Grouping menu. Figure 4-10 shows a Channel Grouping submenu.

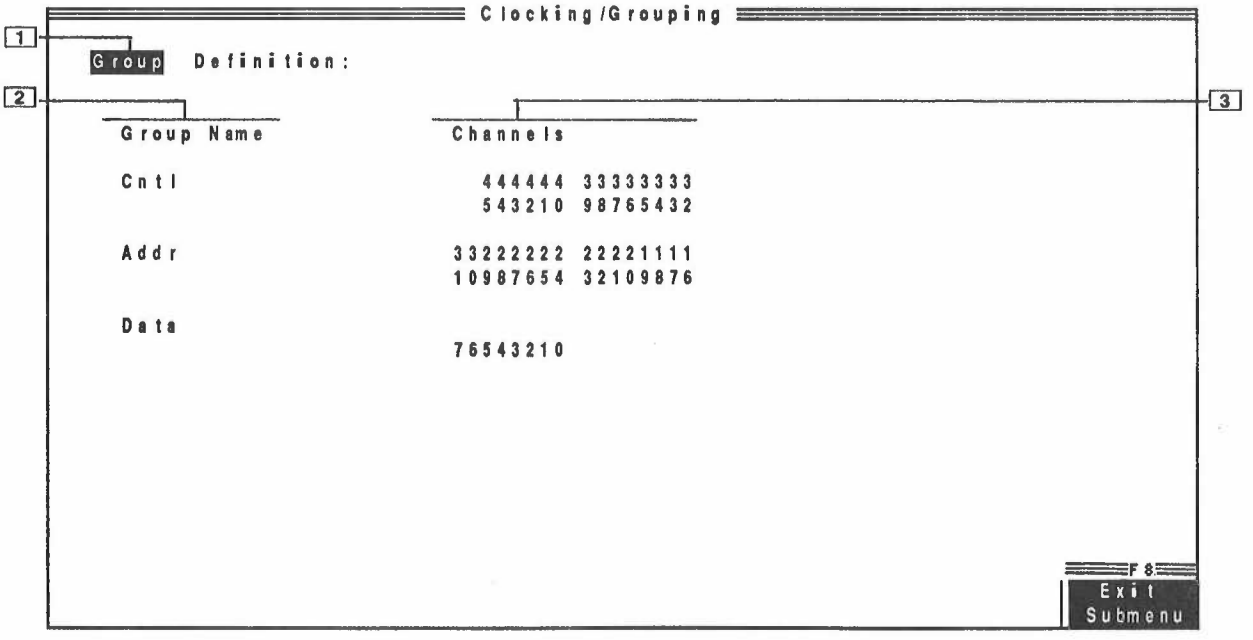


Figure 4-10. Channel Grouping submenu.

1 **Group.** Defines the channel groups.

2 **Group Name.** The disassembler predefines three or more groups, typically, control, address, and data.

3 **Channels.** This section shows which channels are assigned to each group.

Function keys

F8: Exit submenu. Allows you to leave the Channel Grouping submenu.

You can see how the channels are grouped by performing the following steps:

1. Access the State Setup menu by pressing the SETUP key and choosing STATE SECTION.

2. Access the Clocking/Grouping submenu by pressing F6 (Clocking/Channel definition).
3. In the Clocking/Grouping submenu, move the cursor to the Group or Clock Definition field. Press the SELECT key to toggle between Clock and Group definition. Choose Group to see how the channels are grouped.
4. Press F8: Exit Submenu.

Defining Symbols

You can define specific words that the analyzer will recognize. The disassembler loads a table of symbols representing control group values which correspond to cycle types. This information is often helpful in defining a trigger. You can add symbols to this table, or edit or delete existing symbols. You can save defined symbols and load them at another time.

The Symbol Definition menu is accessed through the Edit menu. Figure 4-11 shows a Symbol Definition menu. This screen shows you what symbols have been defined by the disassembler. The disassembler defines many symbols in the control group. Symbols may also be defined in the address and data groups, but the disassembler does not define any symbols in these groups.

When the analyzer interprets symbols, it compares the word against a list of predefined symbols. It is important to note that the analyzer goes in a particular order down the list, and the first predefined symbol that matches the word is assigned to that word. Because many symbols are defined with one or more Don't Cares, many words may match the symbol and more than one symbol may match the word. The analyzer will assign the first symbol that matches the word, even if there are other symbols which may also match the word. Refer to the specific mnemonic disassembly manual for a list of the predefined symbols and the order in which the analyzer compares tham.

For more instructions on how to add, delete, or edit symbols from the symbol table, as well as how to load a symbol table from memory, refer to *Using Symbols* in the PRISM system user's manual.

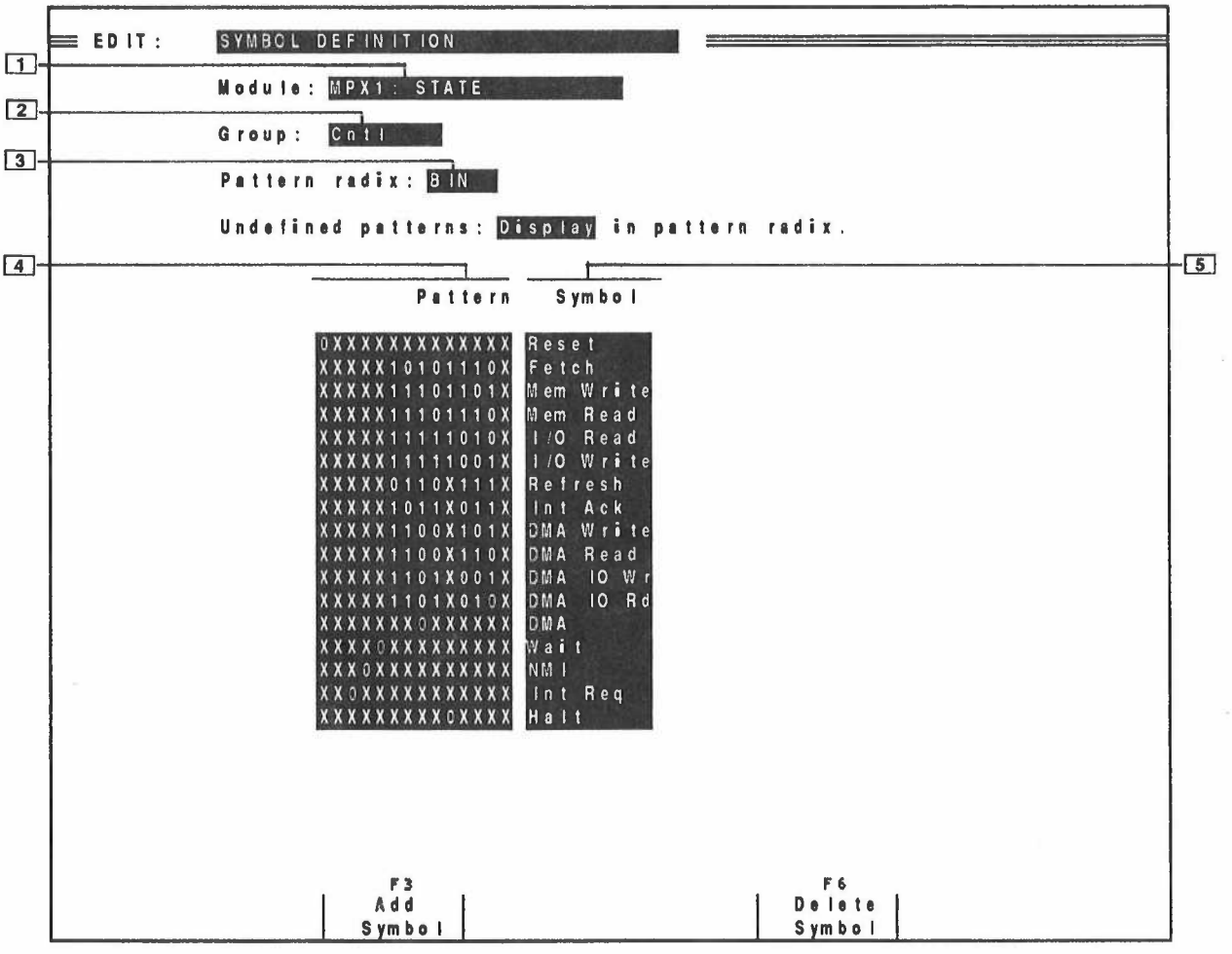


Figure 4-11. Symbol Definition Menu.

1 **Module.** Press SELECT to choose the slot and STATE.

2 **Group.** Press SELECT to choose Control, Address, or Data.

3 **Radix.** Press SELECT to choose BINary, OCTal, or HEXadecimal.

4 **Pattern.** The value of the symbol defined.

5 **Symbol.** The name of the symbol defined.

Defining the Trigger

Having a disassembler connected to the mainframe does not affect the manner in which the trigger is defined. Refer to Setting Up the Trigger in the Using the State Section in this manual for information on how to define the trigger.

Making the Acquisition

After you have defined the trigger specification you are ready to make the acquisition.

Press the Start/Stop key. While the analyzer is acquiring data, the Acquisition Status screen is displayed. This screen keeps you informed of the progress of your acquisition. For information about the Acquisition Status display, refer to the section *Acquiring Data* in your system user's manual.

When the analyzer completes the acquisition, it immediately displays the data stored in the acquisition memory in the State Table display. If the analyzer cannot complete the acquisistion, the Acquisition Status screen will remain on the display. Press the Start/Stop key again to complete the acquisition.

VIEWING DATA WITH A DISASSEMBLER

There are five different formats available to display diassembled data: State, Hardware, Software, Control Flow, and Subroutine. The State display is the same as the state display without a disassembler connected. The other four formats show disassembled mnemonics in a similar format.

State Table

The state table shows the acquisition without being processed by the disassembler.

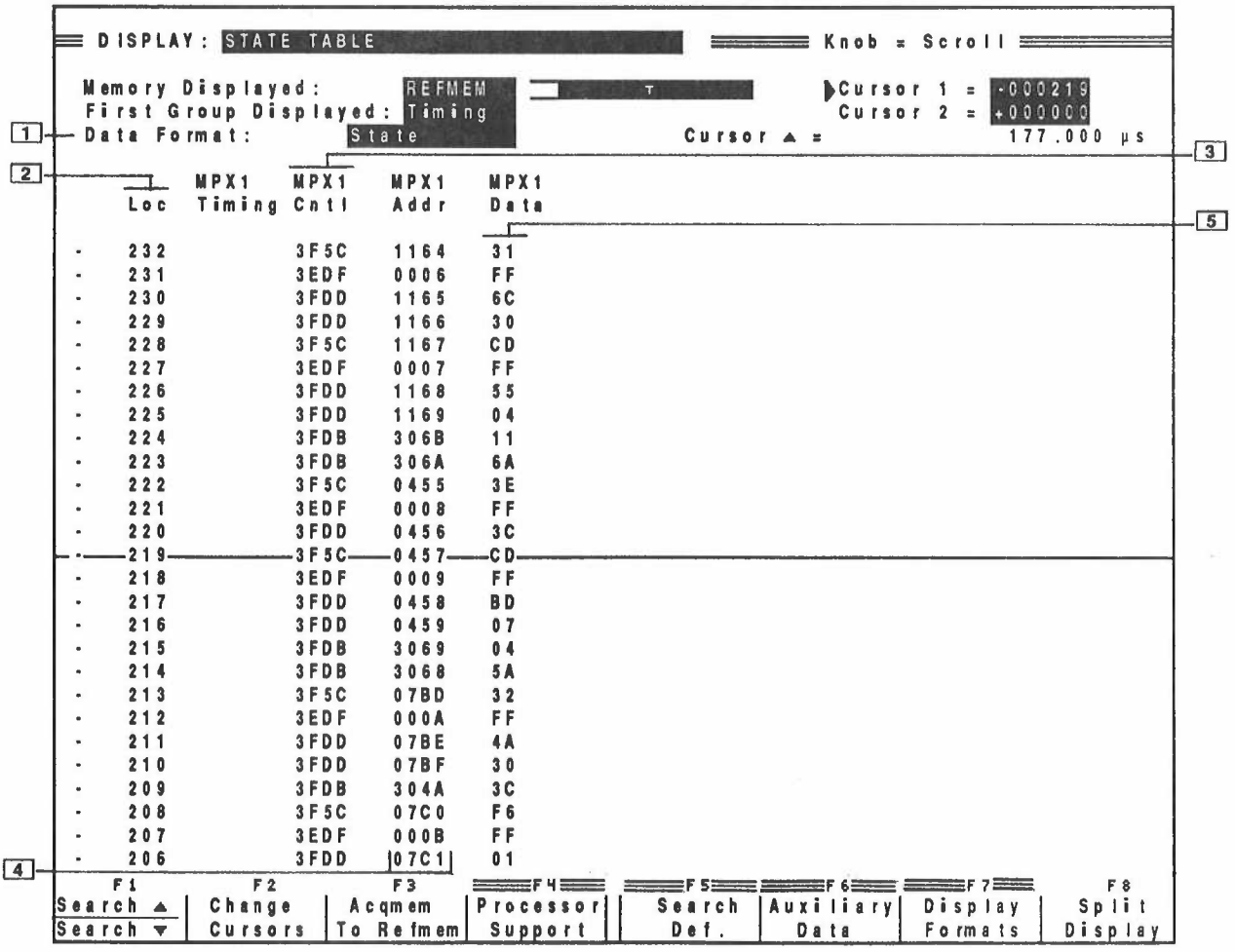


Figure 4-12. State Table Display.

1 **Data Format.** Press the SELECT keys to cycle through the choices. Format choices are: State, Hardware, Software, Control Flow, and Subroutine.

2 **Location Column.** Shows the location in analyzer memory of the data in the line.

3 **Control Group.** Contains channels connected to pins that send and receive control signals.

4 **Address Group.** Contains channels connected to pins that send and receive address signals.

5 **Data Group.** Contains channels connected to pins that send and receive data signals.

Function keys

F4: Processor Support. Use this key to get more information about the specific disassembler that is loaded.

Hardware

The Hardware display shows all the cycles and data acquired. The acquisition is disassembled and the code is listed alongside the other information for each location. Parentheses are used to indicate that the cycle is not a first instruction fetch.

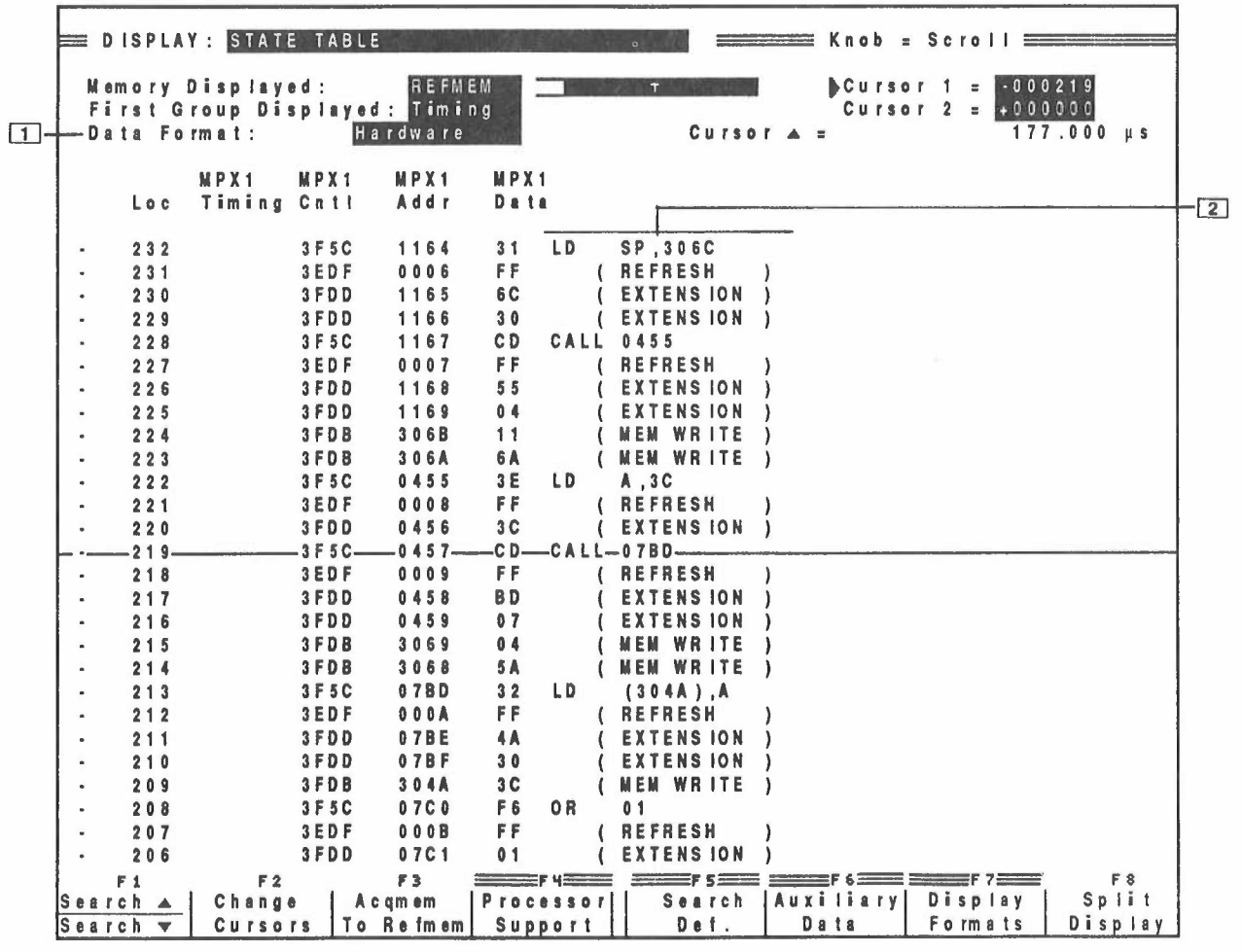


Figure 4-13. Hardware Display.

1 **Data Format.** Identifies this as a hardware display.

2 **Disassembly Mnemonic.** Assembly language instruction or cycle type.

Function keys

F4: Processor Support. Use this key to get more information about the specific disassembler that is loaded.

Software

The Software display suppresses everything but valid instructions. Flushed cycles and extensions are not shown.

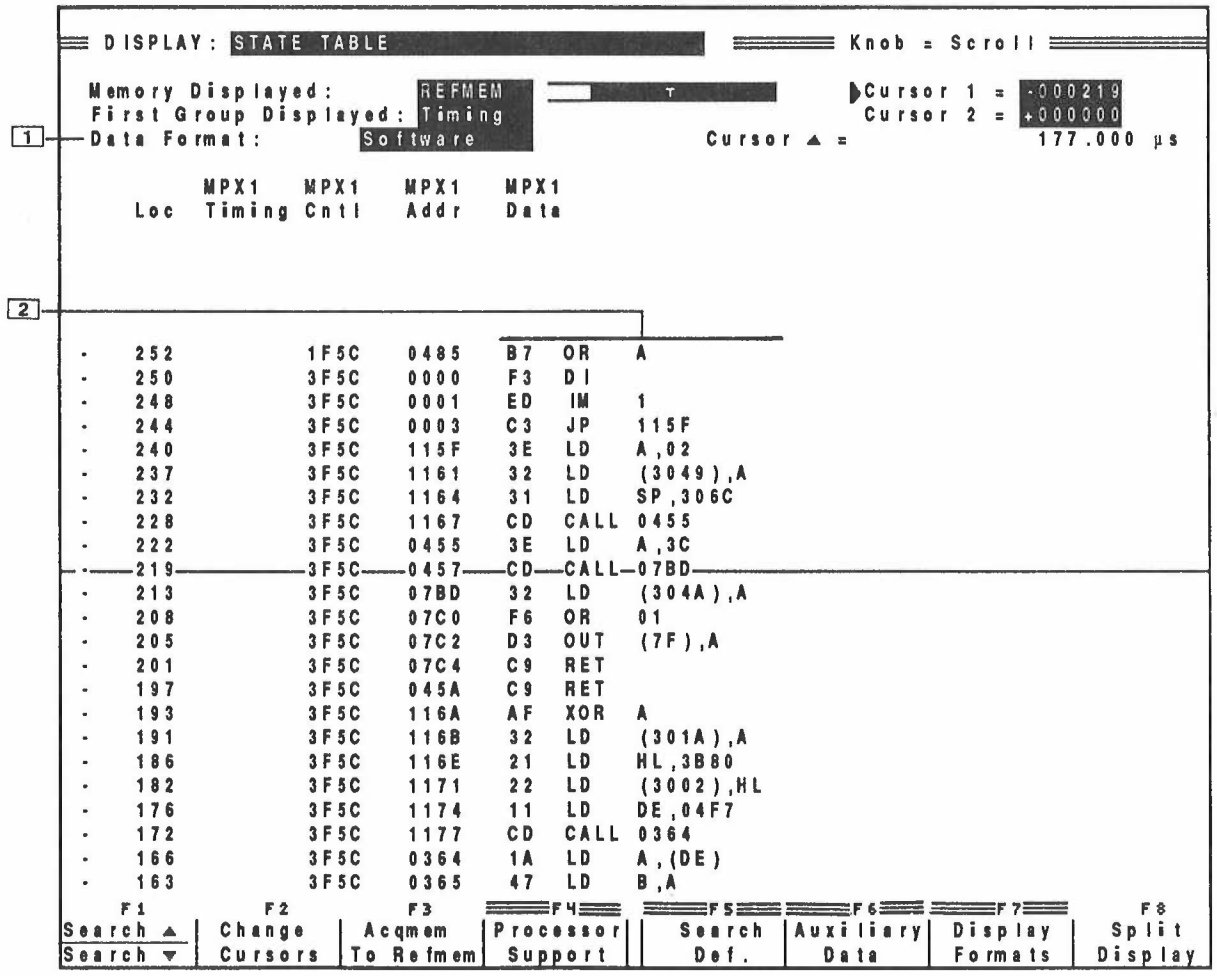


Figure 4-14. Software Display.

1 **Data Format.** Identifies this as a software display.

2 **Disassembly Mnemonic.** Assembly language instruction.

Function keys

F4: Processor Support. Use this key to get more information about the specific disassembler that is loaded.

Control Flow

The Control Flow display shows a subset of the Hardware display. Whether taken or not, the display shows all branches, subroutine calls, and subroutine returns.

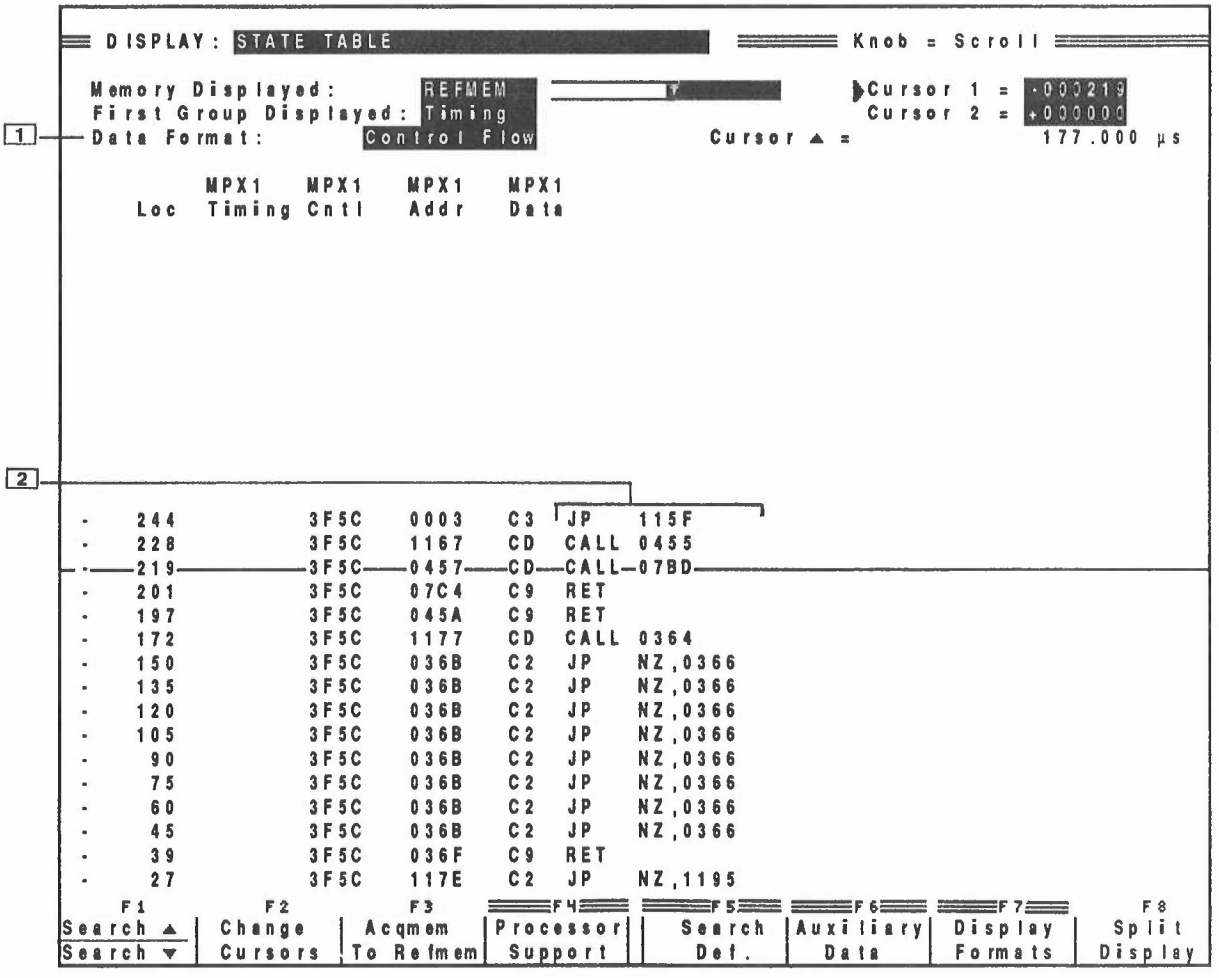


Figure 4-15. Control Flow Display.

1 **Data Format.** Identifies this as a Control Flow display.

2 **Disassembly Mnemonic.** Assembly language instruction.

Function keys

F4: Processor Support. Use this key to get more information about the specific disassembler that is loaded.

Subroutine

The Subroutine display shows an even smaller subset of the Software display. Whether taken or not, the display shows all calls and returns.

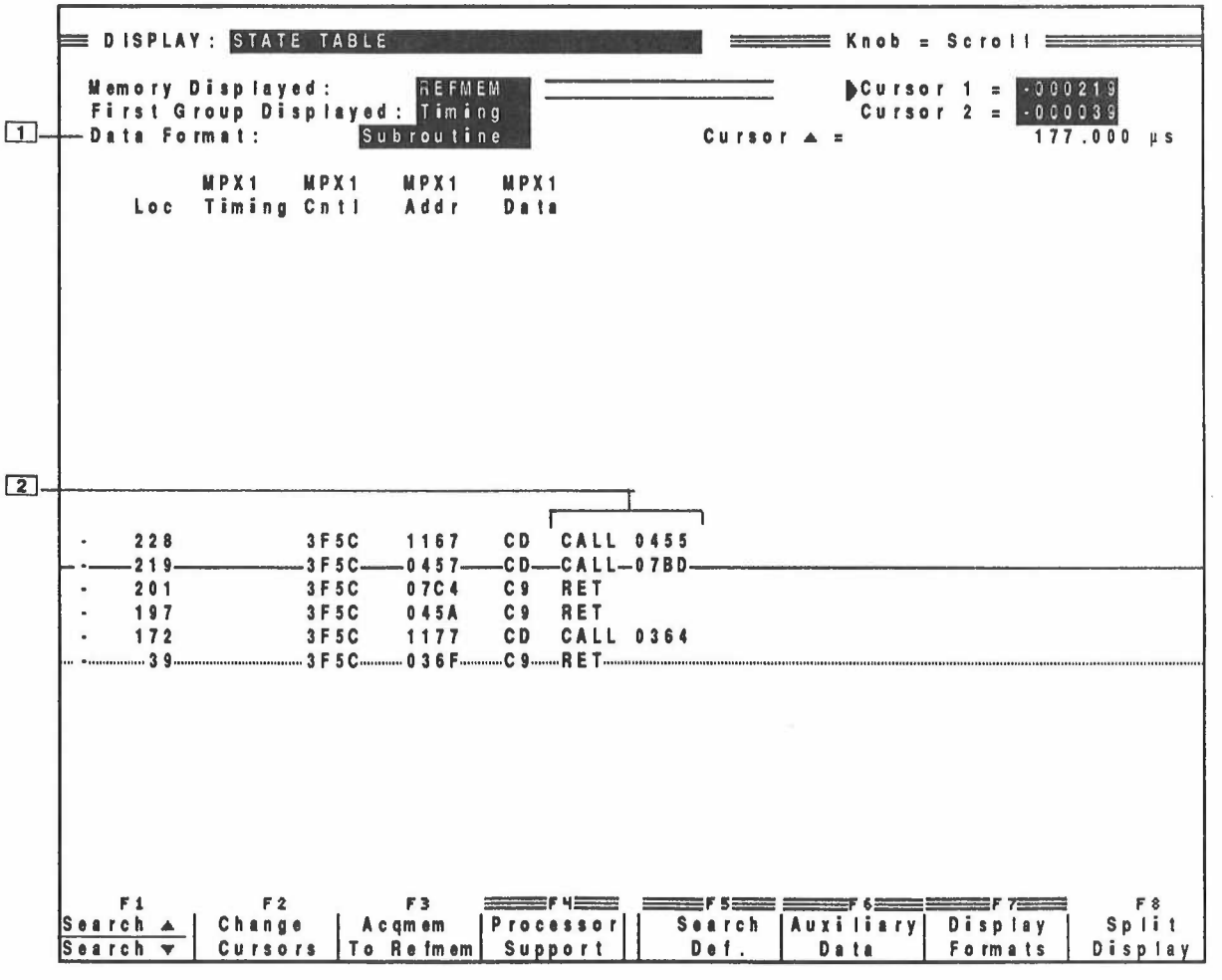


Figure 4-16. Subroutine Display

1 **Data Format.** Indicates Control Flow display

2 **Disassembly Mnemonic.** Assembly language instruction.

Function keys

F4: Processor Support. Use this key to get more information about the specific disassembler that is loaded.

DISPLAY FEATURES

The data display contains some features specific to the disassembler you are using. The disassember uses special characters in the display to indicate abnormalities and certain functions in the disassembled data. The Processor Support submenu contains features specific to the disassembler. The Split Screen display can be used to show two acquisitions at the same time or two sections of the same acquisition.

Special Characters

The disassember uses special characters in the display to indicate abnormalities and certain functions in the disassembled data. The disassembled mnemonic is presented in the display using the conventions of the particular microprocessor being disassembled. In hardware display, opcode extensions are represented in parenthesis.

An asterisk (*) indicates a legal instruction that is missing its operands. The number of asterisks may vary depending on how many digits of operand are missing.

A lower case m appearing before the disassembled mnemonic indicates that the cycle has been marked. For information about marking cycles, see below.

Other special characters may be seen in the display. For descriptions of other special characters, refer to your disassembler manual.

Processor Support

This menu tells you which microprocessor is being disassembled. There are different features available to you, including Mark Cycle. There may be more features available to you which are specific to the particular microprocessor you are disasembling. For descriptions of other processor support features, refer to your mnemonic disassembly manual.

Mark Cycle

You can force the disassembler to reinterpret the data in the acquisition by using mark cycle. With mark cycle, you can select a cycle and tell the disassembler the cycle type you want that cycle to be identified as. Marking opcodes can also change the disassembly of other nearby cycles. If you save an acquisition memory or reference memory to disk, the cycle marking is not restored. After you press F1 to mark a cycle, the disassembler reprocesses the data. The marked cycle is shown in the disassembly mnemonics with a small m before the disassembly mnemonic.

NOTE

The small m will not be displayed in State Table display. You must be in one of the disassembled formats for the m to appear.

You can mark a cycle by performing the following steps:

1. Press F4: Processor Support to access the submenu.
2. Place the cursor on the cycle to be marked.
3. Move the cursor to the Mark current cycle as field.
4. Use the SELECT keys to scroll through the choices, and select the one you want.
5. Press F1: Mark Cycle to mark the cycle.

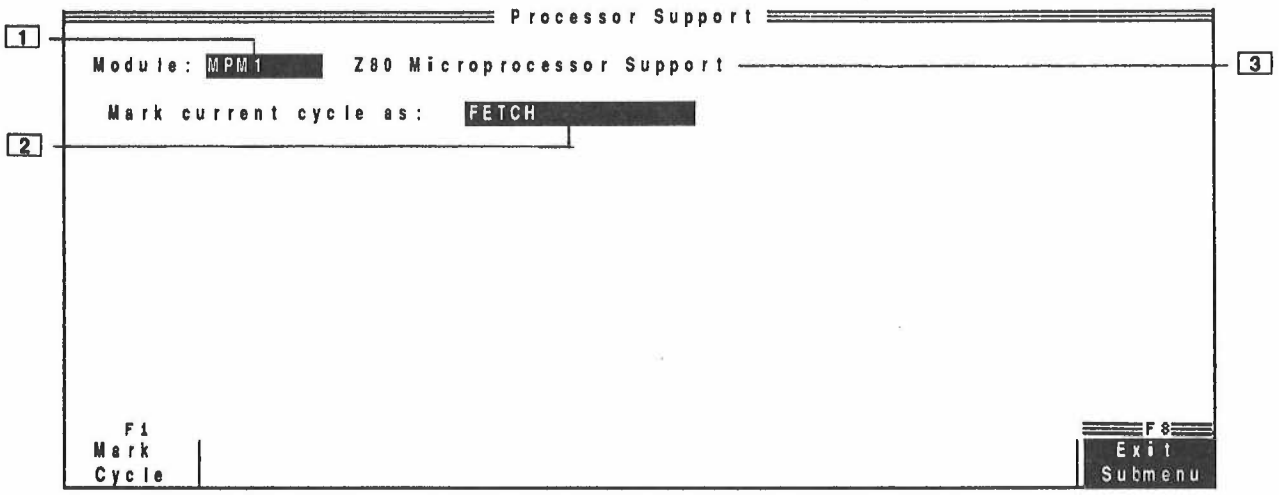


Figure 4-17. Processor Support Submenu.

1 **Module.** Use this field to select the slot.

[2] **Mark current cycle as.** Use the SELECT keys to scroll through the choices. The choices will depend on which microprocessor is being disassembled. Then press F1 to mark the cycle.

[3] **Processor Type.** This field cannot be changed; it is for your information. It identifies which microprocessor is being disassembled.

Function keys

F1: Mark Cycle. Press F1 to perform the mark cycle.

F8: Exit submenu. Allows you to leave the submenu.

Split Screen Display

You can show two acquisitions at the same time, or two sections of the same acquisition by using the split screen function. For more information about this feature, refer to the section *Displaying Data* in the PRISM system user's manual.

When you have two different displays with linked cursors, the cursor will seem to move at different speeds in each of the displays. This is because linked cursor scrolling is based on time, not on location. Since all microprocessor cycles do not take the same amount of time, the cursor in one display might scroll while the cursor in the other display does not.

Section 5: USING THE PROTOTYPE DEBUG TOOL

The prototype debug tool (PDT) represents a new approach to developing processor-based prototype systems. PDT consists of hardware and software that can be used to read and write emulation memory to replace the EPROMs and their contents in your prototype system under test. While the PDT is replacing the EPROMs, you can run and control your microprocessor system to debug your program interactively. When you are satisfied with the emulation memory-resident program, you can copy the program from the PDT memory to a disk file for use in burning final EPROMs.

The General Purpose PDT can be used with any EPROM-based microprocessor system with an 8- 16- or 32-bit wide data bus.

PDT supports your prototype system firmware development because of the wide range of ways the PDT interacts with your prototype system. Using the PDT you can:

- fill, patch, and display the contents of prototype system memory
- reset and stop your prototype system
- download and upload code between your prototype system, the PDT probe, your PRISM RS-232C port, and MS-DOS-compatible disk files
- load and execute software tests for bus, timing and system performance anaylsis
- use other tools available in your PRISM system in conjunction with the PDT

The General Purpose PDT can be used with any system that incorporates EPROMs and uses a microprocessor for which a specific PDT is not available.

A PDT that is designed to work with a specific microprocessor has a monitor program that adds more functionality to the PDT. With a microprocessor-specific PDT you can:

- examine and change register contents
- set and clear software breakpoints
- single step your prototype microprocessor
- examine and change system RAM contents

- set and clear hardware breakpoints

For more information about using a microprocessor-specific PDT, see the user's manual that comes with it.

PDT THEORY OF OPERATION

The process used to develop a ROM-resident application is made easier by using PDT.

When you develop a ROM-resident application you assemble or compile the program code on any host computer using an assembler or cross assembler. At this point in traditional firmware development, you would burn an EPROM and insert it into your prototype system. By using the PDT, you can omit this step. You can transfer the program code to the PDT probe using an MS-DOS format floppy disk or through an RS-232C port on your PRISM mainframe. If you wish, you can burn the EPROM and transfer the program from the EPROM to the PDT probe through the probe adapter socket. The executable image appears in the prototype memory space just as if you had programmed a ROM or an EPROM and plugged it into your prototype.

Next, you insert the PDT probe adapter podlet into the prototype system EPROM socket. The PDT probe adapter is connected to the PDT probe. The PDT probe contains 1 megabit of overlay RAM that replaces the EPROM (thus PDT can emulate EPROMs up to 1 megabit per PDT probe; you can use up to four PDT probes to increase the emulation memory to four megabits). Figure 5-1 shows a PDT configuration.

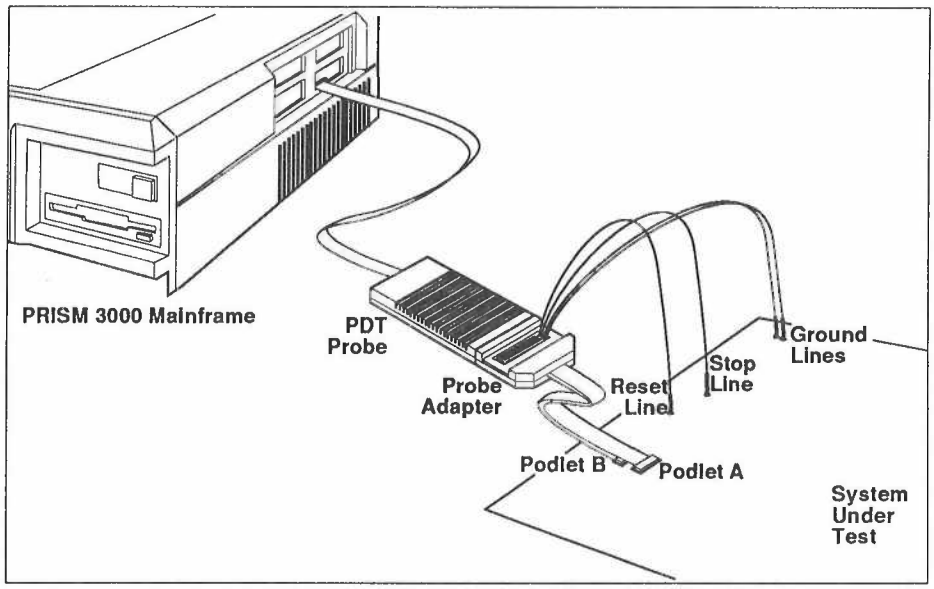


Figure 5-1. A PDT configuration. Podlets A and B replace two EPROMs in the SUT.

The program in the PDT emulation RAM now takes the place of the EPROM. The same RAM can be read and executed by the prototype system, but your prototype will not be able to write to this RAM.

The PDT probe is connected to the MPM application module in the PRISM. You enter a command through the PDT software running on the PRISM. The PDT software processes this information and sends the appropriate command code and data to a location in the RAM on the PDT probe.

Since the PDT probe adapter has replaced the prototype system EPROM, changes to the RAM on the PDT probe will effectively change the contents of what would have been the EPROM in the prototype system. This way, you can interact with the prototype system by changing the contents of the PDT-replaced EPROM. When you are satisfied with the program, the correct code can be copied from the PDT memory to a disk file in order to burn final EPROMs.

PDT speeds up the edit-compile-test cycle by eliminating the need to repeatedly unplug, erase, re-burn, and re-socket EPROMs. You will need to burn an EPROM once only after you have debugged and tested your code.

STEPS TO USE THE PDT

Using the PDT the first time requires that you to perform five steps. References to sections of this manual follow the brief overview of the steps to run the PDT

1. Install the PDT Software

Installing the PDT software involves copying files from your PDT software disk to the support directory of your boot disk. Instructions for installing the PDT software on a hard-disk and a floppy-disk system will be found in the appendix *Installing PDT*.

2. Set Up the PDT Configuration Submenu

You must set up the PDT probe based on the type and number of EPROMs the PDT will replace along with the bus width of your prototype system and the EPROM starting address. You make these selections in the PDT Configuration submenu. After you have made these selections, the submenu will display a correlation between each EPROM in your prototype system and a PDT probe and podlet. Information about the PDT Configuration submenu will be found in the section *Setting Up the PDT Menus*.

3. Make Hardware Connections

Your hardware must be configured to correspond with the selections you made in the PDT Configuration submenu. Based on the information in the submenu, connect the correct probe adapter to the PDT probe and the correct podlet to your SUT. Instructions for making hardware connections will be found in the appendix *Installing PDT*.

4. Load Program into PDT

In order to have the PDT replace the EPROMs in your prototype system, you must have the EPROM program loaded in the PDT. You can load a program from the EPROM itself, from a MS-DOS compatible disk file, or from the PRISM RS-232C port. Instructions for loading programs into the PDT will be found in the section *Loading and Saving Programs*.

5. Debug Your Program

Now you are ready to debug your program. You can interact with your prototype system by typing in PDT commands. You can dump memory contents, patch locations, start and stop your prototype. Information about the various PDT commands will be found in the section *PDT Commands*.

ADVANTAGES OF USING PDT

Microprocessor emulators generally acquire data synchronously. PDT can work with other modules in the PRISM system so that you can acquire timing information both synchronously and asynchronously. The data can be displayed as a graphic timing diagram. This allows you to look at transitions, events and timing without being limited by system clocking restrictions.

The PDT allows you to debug your program in real time. There are no emulator wait states to degrade the prototype system's performance. Because the PDT is part of the PRISM system, you have a logic analyzer available to give you timestamped, fully correlated data.

APPLICATIONS FOR PDT

PDT complements a PDT state acquisition probe. Together they perform many of the functions of a microprocessor emulator.

You can use PDT to do the following:

- debug, integrate or validate operating system kernels, device drivers, firmware packages, I/O ports, peripherals, and multiprocessor and real-time embedded sytems
- develop and debug ROM-resident programs for embedded microprocessor systems
- develop and debug system software
- test and troubleshoot your hardware
- save and edit ROM-resident code using MS-DOS compatible 3.5-inch floppy disks
- download and execute code from MS-DOS compatible floppy disk or through a RS-232C port
- control your prototype by toggling an interrupt or control line during state or timing data acquisition

PDT may be used with other PRISM system tools to manipulate the memory of a system under test.

Appendix A
INSTALLING SOFTWARE

You must intall the software which came with the MPM application module. If you have a hard drive in your PRISM, follow the Hard Drive directions. If you do not have a hard drive in your PRISM, use the Floppy Drive directions.

You will receive a floppy disk with your MPM application module. There will be two directories on the floppy disk: Device and Support.

Hard Drive

Perform the following steps to install the MPM software in your PRISM system:

1. Use the Copy Directory command to copy the files in the Device directory of the MPM floppy disk to the Device directory on your hard drive. For information about the Copy Directory command, refer to the section Using Utilities in your system user's manual.
2. Use the Copy Directory command to copy the files in the Support directory of the MPM floppy disk to the Support directory on your hard drive.

Floppy Drive

Perform the following steps to install the MPM software in your system floppy disks:

1. Use the Copy File command to copy the files in the Device directory of the MPM floppy disk to the Device directory on your Applications floppy disk. For information about the Copy File command, refer to the section Using Utilities in your system user's manual.
2. Use the Copy File command to copy the files in the Support directory of the MPM floppy disk to the Support directory on your Applications floppy disk.

INSTALLING HARDWARE

If you ordered your MPM application module when you ordered your system, the PRISM will arrive with the module already installed. If you ordered your MPM application after you ordered your PRISM, you must have a qualified service technician install the application module in your PRISM mainframe.

WARNING

Serious electric shock hazards exist within the mainframe. Do not remove covers. Installation of application modules should only be performed by a qualified service technician. Instructions for application module installation are in the Mainframe Service Manual.

Appendix B
SPECIFICATIONS

This section lists two types of specifications: (1) those that are classified as functional, environmental, physical, or "static" specifications (specifications that cannot be verified by the user); and (2) those that are actual operational parameters (performance specifications that are user-verifiable). Refer to Verification and Adjustment procedures in Section 5 for procedures that verify the performance specifications.

The following terms are used in the specification tables:

Characteristic: A property of the product.

Performance Requirement: The primary performance characteristics of the product that can be verified using verification procedures.

Supplemental Information: Statements that describe typical performance for characteristics of secondary importance (those that are not usually verified using verification procedures) or statements that further explain related performance requirements.

CHARACTERISTICS/SPECIFICATIONS

The performance characteristics in this section are valid under the following conditions:

1. The 30MPM/MPX Application Modules and associated probes must be operating in an environment as specified in Table B-1 of the applicable Mainframe service manual.
2. A warm-up period of at least 20 minutes must precede the verification/operational procedures.

The following tables list the specifications and performance characteristics of the 30MPM and 30MPX Application Modules, P6480 Probe, P6486 Probe, and associated leadsets. The GPPA (general purpose) leadset complies with the P6480 Probe environmental and safety specifications. The standard and high-performance leadsets comply with the P6486 Probe environmental and safety specifications.

Table B-1
30MPM/MPX FUNCTIONAL REQUIREMENTS

Characteristic	Description
STATE SECTION	
Number of Probe Input Channels Supported	64 maximum (30MPM) 96 maximum (30MPX)
Microprocessor Support	8/16 bit (30MPM) 8/16/32 bit (30MPX)
Clocking Modes	Refer to the P6480 specifications in Table B-7
PROBE INTERFACE:	
30MPM 30MPX	16 channels 32 channels
Bus Cycle Rate (maximum)	
30MPM	12.12 MHz (82.5 ns) with 64 probe input channels or 16.00 MHz (62.5 ns) with 48 probe input channels
30MPX	16.00 MHz (62.5 ns) with 96 probe input channels
ACQUISITION MEMORY:	
Size	8192 samples, each consisting of: 44-bit timestamp 1 trigger bit plus 3 other flag bits 64 acquisition channels (30MPM) or 96 acquisition channels (30MPX)
Depth	A single acquisition can fill all, 1/2, 1/4, 1/8, or 1/16 of memory.
Partitions	1, 2, 4, 8, or 16 equal partitions
Trigger Mode	Trigger immediately
Trigger Position	One of five user-selectable positions: 97%, 75%, 50%, 25%, or 3% postfill (the trigger position determines how many samples will be stored after a trigger occurs)
Storage Qualification	Global (based on condition list) Sequential (accomplished with start storage, stop storage, and store sample general actions)

(Table continued on next page)

Table B-1 (Con't.)
30MPM/MPX FUNCTIONAL REQUIREMENTS

Characteristic	Description
TRIGGERING:	
Control Sequence	Consists of 1 to 7 states (state 0 through state 6) plus a trigger state (state 7). Each state performs condition tests on the input data. If the tests are satisfied, then one or more actions are executed.
Number of Tests per State	1 - 8 (except for state 7, the trigger state)
Test Linkage	Boolean AND/OR of up to 4 Conditions
Test Evaluations	Wait For/Wait For Not or If/If Not
Test Occurrence Counter Range	1 to 65,535
General Actions per Test	0 - 13 (14 with PDT option)
State Control Actions per Test	1
Condition Types	8 range/equivalence recognizers (6 with PDT running) 8 counter/timers (7 with performance analysis running) 4 Intermodule Signal lines (SIGNAL[1:4])
Range/Equivalence Recognizer Output Conditions	True as defined or true as complemented
Counter/Timer Test Conditions	< or ≥
Counter Range	1 to 2,147,483,647
Timer Range	60 ns to 42.94967294 seconds, with 20 ns resolution Note: A timer condition cannot be detected as false for 120 ns or true for 140 ns after restarting or resuming timer. Also, timer limit tests occur only when a state machine instruction occurs; therefore, an expired timer will not be detected until the next sample is received.
SIGNAL[1:4] Conditions	True as set or true as clear (may be monitored or driven) Note: TekEvent tests occur only when a state machine instruction occurs; therefore, an event will not be detected until the next sample is received.

(Table continued on next page)

Table B-1 (Con't.)
30MPM/MPX FUNCTIONAL REQUIREMENTS

Characteristic	Description
General Actions	
Counter/Timer	Reset Counter Increment Counter Resume Timer Restart Timer Stop Timer
Store	Store Sample Start Storage Stop Storage
TekEvent Signal Lines	Set Signal Clear Signal
Assert Stop	Available only when PDT is installed
Sequence Actions	Trigger State section Trigger System GOTO State N (N = the desired state number) Begin Again (restarts state machine) Do Nothing
Other Trigger Resources	1 System Trigger line
TIMING SECTION	
PROBE INTERFACE:	10 channels: 9 data and 1 synchronous clock input
Clocking	Input data transition or sync clock. Rising or falling clock edge may be selected.
Sampling Rate	
Transition Mode	200 MHz (When using a P6486 Probe with a high-performance leadset)
Synchronous Mode	90 MHz (When using a P6486 Probe with a high-performance leadset)

(Table continued on next page)

Table B-1 (Con't.)
30MPM/MPX FUNCTIONAL REQUIREMENTS

Characteristic	Description
ACQUISITION MEMORY:	
RAM Size	1K X 20-bits (data and timestamp shared storage). Each location consists of: Data/Timestamp flag bit and two 9-channel data samples or one 19-bit timestamp (during post-acquisition, the timestamp is 20-bits wide with no flag bit)
Acquisition Depth	2048 transition samples
TRIGGERING:	
Internal Resource	One 9-bit word recognizer (selectable output polarity) 1 of 4 Signal lines
Word Recognizer Sample Rate	200 MHz
Trigger Tests	Event (word recognizer) Event and Signal
Trigger Actions	Trigger Section Trigger System Trigger Section and Set Signal Trigger System and Set Signal
Trigger Positioning	One of five user-selectable trigger positions in RAM: 97%, 75%, 50%, 25%, or 3% postfill (the trigger position determines how many samples will be stored after a trigger occurs)
Other Trigger Resources	1 System Trigger line
COMMUNICATION SECTION	
Intermodule Interface	4 Signal Interface lines 1 System Trigger line
ADDITIONAL FEATURES	Supports Prototype Debug Tool (PDT) option (Refer to PDT manuals for more information about PDT functions)

Table B-2
30MPM/MPX PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
STATE SECTION		
Delay from P6480 Probe Tip to Trigger Machine Test		
30MPX 30MPM (48 channels) 30MPM (64 channels)		310 ns to 410 ns 310 ns to 410 ns 330 ns to 430 ns
Delay from Timer True to Trigger Machine Detection		140 ns minimum (A timer will go true and be seen as true in 1 bus cycle if the bus cycle time is at least 140 ns.)
Delay from Timer Restart to Timer Condition Forced False		120 ns (A timer which is true will be forced false 120 ns after Restart command. Begin Again and New Partition force timers false by the first bus cycle following action.)
Delay from Intermodule Signal Sampled to Trigger Machine Test		60 ns minimum
Delay From Trigger Machine Test to Intermodule Signal Driven on Bus		200 to 260 ns
Delay from System Trigger Sampled to Trigger Machine Test		60 ns minimum
Delay from Trigger Machine Test to System Trigger Line Driven on Bus		200 to 260 ns

(Table continued on next page)

Table B-2 (Con't)
30MPM/MPX PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
TIMING SECTION		
Maximum Input Data Rate	100 Mbits/sec	Measured using P6486 Probe with high-performance leadset. Verified by P6486 verification procedures.
Maximum External Sync Clock Rate	90 MHz	Measured using P6486 Probe with high-performance leadset. Verified by P6486 verification procedures.
Word Recognizer Sample Rate	200 MHz (5 ns resolution)	Verified by Timing diagnostic routines
Delay from P6486 Probe Tip to Signal Line Assertion		140 ns ±50 ns
Delay from P6486 Probe Tip to System Trigger Line Assertion		140 ns ±50 ns
Delay from Signal Line Input to Timing Section Trigger		45 ns ±10 ns
Delay from System Trigger Input to Timing Section Trigger		25 ns ±10 ns

Table B-3
30MPM/MPX ENVIRONMENTAL SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Temperature		Meets MIL-T-28800C, class 5
Operating	0 to +50° C	
Non-operating	-55 to +75° C	
Thermal Switch Threshold	85° C	Switch closes when temperature exceeds 85° C.
Relative Humidity	10% to 95%	Meets MIL-T-28800C, class 5
Altitude		Meets MIL-T-28800C, class 3
Operating	4.5 Km (15,000 ft)	
Non-operating	15 Km (50,000 ft)	
Vibration	0.38 mm (.015") @ 10 Hz to 55 Hz	Meets or exceeds MIL-T-28800C, class 5
Shock	30 Gs @ 11 ms	Meets MIL-T-28800C, class 3
Electrostatic Discharge	20 KV through 500 Ω resistor with 500 pF capacitor	Tested in 3001 & 3002 Mainframes. No component failure.

Table B-4
30MPM/MPX PHYSICAL SPECIFICATIONS

Characteristic	Description
Product Dimensions	
Length	14.825 inches (37.656 cm)
Width	10.200 inches (25.908 cm)
Weight	1.6 lbs (0.7 Kg) approximate weight

Table B-5
30MPM/MPX SAFETY AND REGULATORY SPECIFICATIONS

Characteristic	Description
Safety	Complies with UL 1244, CSA 556B, IEC 348 when used in a 3001/3002 Mainframe
Designed Operation	Low-voltage, low power. Less than 42.4 VAC or 60 VDC between any two terminals. Less than an additional 150 watts available.
Electromagnetic Compatibility (EMI)	VDE 0871, level B (without probes or CommPack cable attached)

Table B-6
30MPM/MPX RELIABILITY SPECIFICATIONS

Characteristic	Description
Mean Time Between Failure (calculated value)	
30MPM	6700 hours
30MPX	6400 hours

Table B-7
P6480 STATE PROBE FUNCTIONAL REQUIREMENTS

Characteristics	Description
Input Channels	96, split into thirteen groups: CH[3:0] CH[7:4] CH[15:8] CH[23:16] CH[31:24] CH[39:32] CH[47:40] CH[55:48] CH[63:56] CH[71:64] CH[79:72] CH[87:80] CH[95:88]
Clocking Modes	Asynchronous Synchronous (all groups logged in by single-phase clock) Demux (two alternating phases, each with independent clock edge) Microprocessor-specific
Synchronous Clock Rate	33.3 MHz (30 ns) maximum (single edge)
Clock Inputs	3
Maximum Clock Phases	2
Clocking RAM	4K X 8 bits
Asynchronous Clock Timebase	100 ns to 500 ms (1-2-5 sequence)
Qualifier Inputs	8
Bus Cycle Rate (maximum)	
30MPM	12.12 MHz (82.5 ns) with 64 probe input channels or 16.00 MHz (62.5 ns) with 48 probe input channels
30MPX	16.00 MHz (62.5 ns) with 96 probe input channels
Retargetable	The P6480 is adapted to different processor and package styles by a replaceable leadset

Table B-8
P6480 STATE PROBE PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
ACQUISITION INPUTS CH[95:0]:		
Input Capacitance		40 pF (Does not include leadset)
Input Voltage Limits		0 V-0 8 V (low) 2.0 V-5.25 V (high)
Threshold Voltage	1.4V ±0.5 V	Not variable
Setup/Hold Times	15 ns/0 ns (default value) 8 ns/8 ns* 0 ns/15 ns*	Setup/hold tolerance: ±3 ns *These values are determined by microprocessor leadset used and are not verified
Minimum Clock Width	10 ns (single edge)	
Minimum Time Between Active Clock Edges	30 ns	

Table B-9
P6480 PROBE ENVIRONMENTAL SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Temperature		
Operating	0 to +50° C	
Non-operating	-55 to +75° C	
Humidity		
Operating and non-operating	10% to 95% relative humidity maximum	
Altitude		Exceeds MIL-T-28800D, class 3
Operating	4.5 Km (15,000 ft)	
Non-operating	15 Km (50,000 ft)	
Vibration	0.64 mm (0.025") @ 10 Hz to 55 Hz P-P for 75 minutes total	Meets or exceeds MIL-T-28800D, class 3
Shock	50 Gs @ 11 ms	MIL-T-28800D, class 3
Bench Handling Drop Test	Drop from height of 91 cm (3 ft.); 3 drops on each side (18 total)	Meets or exceeds MIL-T-28800C, class 3
Electrostatic Discharge	6 KV through 200 Ω resistor with 500 pF capacitor	

Table B-10
P6480 PROBE PHYSICAL SPECIFICATIONS

Characteristic	Description
Probe Dimensions (approximate)	
Length	6.0 inches (15.2 cm)
Width	4.2 inches (10.6 cm)
Height	1.15 inches (2.92 cm)
Cable Length	79 inches (2 meters) from probe to Module
Weight	1 lb (0.45 Kg)

Table B-11
P6480 PROBE SAFETY AND REGULATORY SPECIFICATIONS

Characteristic	Description
Safety	Complies with UL1244, CSA 556B when used with an PRISM 3000 Series Mainframe
Designed Operation	Low-voltage, low power. Less than 42.4 VAC or 60 VDC between any two terminals. Less than an additional 150 watts available.
Electromagnetic Compatibility (EMI)	Probes are exempt from VDE per German Postal Regulation 1046/1984 Par. 2, Sect. 1.7.1

Table B-12
P6480 PROBE RELIABILITY SPECIFICATIONS

Characteristic	Description
Mean Time Between Failure	29,750 hours (Calculated value)

Table B-13
GPPA LEADSET PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
Number of Signal Conductors		96
Number of Ground Conductors		18
Typical Loading Capacitance		
Channels 0-7		<65 pF
Channels 8-95		<48 pF
Maximum Loading Capacitance		
Channels 0-7		<90 pF
Channels 8-95		<83 pF

Table B-14
GPPA LEADSET PHYSICAL SPECIFICATIONS

Characteristics	Description
Leadset Dimensions	
Case length	3.0 inches (7.6 cm)
Case width	4.2 inches (10.6 cm)
Case height	1.15 inches (2.9 cm)
Lead length	12.75 inches (32.38 cm) approximate length
Weight	0.56 lbs (0.25 Kg)

Table B-15
GPPA LEADSET RELIABILITY SPECIFICATIONS

Characteristics	Description
Mean Time Between Failure	190,000 hours @ 25° C (Calculated value)

Table B-16
P6486 HIGH-SPEED PROBE FUNCTIONAL REQUIREMENTS

Characteristics	Description
Channels	10
Number of Input Ground Lines	10 with high-performance leadset 2 with standard leadset
Acquisition Modes	Synchronous and Transitional
Acquisition Rate	
Synchronous	90 MHz maximum
Transitional	200 Mhz maximum
Synchronous Clock Inputs	1

Table B-17
P6486 HIGH-SPEED PROBE PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
INPUT LINES (SIG[9:0]):		
Input Bandwidth		
High-Perf. Leadset	200 MHz (3dB point)	
Standard Leadset	100 MHz (3dB point)	
Attenuation Ratio		
High-Perf. Leadset	3 to 1 (3 V at input becomes 1 V at output)	
Standard Leadset	6 to 1 (6 V at input becomes 1 V at output)	
Minimum Data Word Width to Guarantee Sample		
High-Perf. Leadset	6.0 ns	
Standard Leadset	7.5 ns	
Channel-to Channel Skew		
High-Perf. Leadset	<0.5ns	
Standard Leadset	<2.0 ns	

(Table continued on next page)

Table B-17 (Con't.)
P6486 HIGH-SPEED PROBE PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
Threshold Range (relative to reference lines)		
High-Perf. Leadset	-5.0 V to +5.0 V	
Standard Leadset	-10 V to +10 V	
Threshold Accuracy		
High-Perf. Leadset		±50 mV
Standard Leadset		±100 mV
Threshold Step Size		
High-Perf. Leadset		25 mV
Standard Leadset		50 mV
Minimum Drive Above Threshold		
High-Perf. Leadset		200 mV
Standard Leadset		300 mV
Input Voltage Range		
High-Perf. Leadset		-6 V to +6 V about threshold
Standard Leadset		-12 V to +12 V about threshold
Input Resistance		
High-Perf. Leadset		100 KΩ nominal
Standard Leadset		165 KΩ nominal
Input Capacitance		
High-Perf. Leadset		11 pF
Standard Leadset		<11 pF
Input Bias Current		<30 µA (both leadsets)
Non-Destructive Input Voltage Range (estimate)		±50 V maximum (both leadsets)

(Table continued on next page)

Table B-17 (Con't.)
P6486 HIGH-SPEED PROBE PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
REFERENCE LINES (REF[9:0])		
Input Reference Range		
High-Perf. Leadset Standard Leadset		-10 V to +15 V -25 V to +25 V
Input Resistance		>20 MΩ (capacitively coupled)
Input Capacitance		1000 pF ±10%
SYNCHRONOUS CLOCKING:		
Maximum Clock Rate	90 MHz (single edge)	
Minimum Time Between Active Clock Edges	11 ns	
Minimum Clock Width	2.0 ns (single edge)	
Data Setup/Hold Time	1.5 ns/1.0 ns 2.5 ns/1.0 ns	With high-performance leadset With standard leadset

Table B-18
P6486 HIGH-SPEED PROBE ENVIRONMENTAL SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
Temperature		
Operating	-15° to +55° C	Meets MIL-T-28800C, class 3
Non-operating	-62° to +85° C	
Humidity		Exceeds MIL-T-28800C, class 3
Operating and non-operating	5% to 95% Relative Humidity	
Altitude		Exceeds MIL-T-28800C, class 3
Operating	4.5 Km (15,000 ft)	
Non-operating	15 Km (50,000 ft)	
Vibration	0.635 mm (0.025") @ 10 Hz to 55 Hz P-P for 75 minutes total	Meets or exceeds MIL-T-28800C, class 3
Shock	50 Gs @ 11 ms	MIL-T-28800C, class 3
Bench Handling Drop Test	Drop from height of 91 cm (3 ft.); 3 drops on each side (18 total)	Meets or exceeds MIL-T-28800C, class 3
Electrical Discharge	17 KV through a 1 KΩ resistor in series with a 500 pF capacitor	

Table B-19
P6486 HIGH-SPEED PROBE PHYSICAL SPECIFICATIONS

Characteristics	Description
Probe Dimensions (approximate)	
Length	4.3 inches (10.9 cm)
Width	3.0 inches (7.6 cm)
Height	0.7 inches (1.8 cm)
Cable Length	80 inches (2 meters) ±10% from probe to Module
Weight	10.5 ounces (0.3 Kg) with Module interface cable

Table B-20
P6486 HIGH-SPEED PROBE SAFETY AND REGULATORY SPECIFICATIONS

Characteristics	Description
Safety	Complies with UL 1244, CSA 556B, when used with an PRISM3000 Mainframe
Designed Operation	Designed to operate using low-voltage, low-power signals (less than 42.4 VAC or less than 60 VDC between any two terminals and less than an additional 150 watts available)
Electromagnetic Compatibility (EMI)	Probes are exempt from VDE per German Postal Regulation 1046/1984 Par. 2, Sect. 1.7.1

Table B-21
P6486 HIGH-SPEED PROBE RELIABILITY SPECIFICATIONS

Characteristics	Description
Mean Time Between Failure	>20,000 hours (Calculated value)

Table B-22
STANDARD LEADSET PHYSICAL SPECIFICATIONS

Characteristics	Description
Leadset Dimensions	
Case length	3.0 inches (7.6 cm)
Case width	1.5 inches (3.8 cm)
Case height	0.7 inches (1.7 cm)
Lead length	9.0 inches (22.8 cm)
Weight	2.0 ounces (56.8 Kg)

Table B-23
STANDARD LEADSET RELIABILITY SPECIFICATIONS

Characteristics	Description
Mean Time Between Failure	20,000 hours (Calculated value)

Table B-24
HIGH-PERFORMANCE LEADSET PHYSICAL SPECIFICATIONS

Characteristics	Description
Leadset Dimensions	
Case length	1.75 inches (4.45 cm)
Case width	3.0 inches (7.6 cm)
Case height	0.69 inches (1.75 cm)
Lead length	12 inches (30.5) approximate length
Weight	2 ounces (57 grams)

Table B-25
P6480 PIN-TO-MPM/MPX CHANNEL

Pin Number	Description
A1	Leadset identification line 3
A2	Leadset identification line 0
A3	Leadset input channel 92
A4	Leadset input channel 89
A5	Leadset input channel 85
A6	Leadset input channel 82
A7	Leadset input channel 78
A8	Leadset input channel 75
A9	Leadset input channel 71
A10	Leadset input channel 68
A11	Leadset input channel 64
A12	Leadset input channel 61
A13	Leadset input channel 57
A14	Leadset input channel 54
A15	Leadset input channel 50
A16	Leadset input channel 15
A17	Leadset input channel 11
A18	Leadset input channel 8
A19	Leadset input channel 5
A20	Ground
A21	Leadset input channel 21
A22	Leadset input channel 43
A23	Leadset input channel 40
A24	Leadset input channel 36
A25	Leadset input channel 33
A26	Leadset input channel 29
A27	Leadset input channel 26
A28	Leadset input channel 22
A29	Leadset input channel 19
A30	System ground
B1	Leadset identification line 4
B2	Ground
B3	Leadset input channel 93
B4	Leadset input channel 90
B5	Leadset input channel 86
B6	Ground
B7	Leadset input channel 79
B8	Leadset input channel 76
B9	Leadset input channel 72
B10	Ground
B11	Leadset input channel 65
B12	Leadset input channel 62
B13	Leadset input channel 58
B14	Ground
B15	Leadset input channel 51
B16	Leadset input channel 58
B17	Leadset input channel 12
B18	Ground
B19	Leadset input channel 6

(Table continued on next page)

Table B-25 (Con't.)
P6480 PIN-TO-MPM/MPX CHANNEL

Pin Number	Description
B20	Leadset input channel 2
B21	Leadset input channel 0
B22	Leadset input channel 44
B23	Ground
B24	Leadset input channel 37
B25	Leadset input channel 34
B26	Leadset input channel 30
B27	Ground
B28	Leadset input channel 23
B29	Leadset input channel 20
B30	Leadset input channel 16
C1	Leadset identification line 5
C2	Leadset identification line 1
C3	Leadset input channel 94
C4	Ground
C5	Leadset input channel 87
C6	Leadset input channel 83
C7	Leadset input channel 80
C8	Ground
C9	Leadset input channel 73
C10	Leadset input channel 69
C11	Leadset input channel 66
C12	Ground
C13	Leadset input channel 59
C14	Leadset input channel 55
C15	Leadset input channel 52
C16	Ground
C17	Leadset input channel 13
C18	Leadset input channel 9
C19	Leadset input channel 7
C20	Leadset input channel 3
C21	Ground
C22	Leadset input channel 45
C23	Leadset input channel 41
C24	Leadset input channel 38
C25	Ground
C26	Leadset input channel 31
C27	Leadset input channel 27
C28	Leadset input channel 24
C29	Ground
C30	Leadset input channel 17
D1	+5 V from the probe
D2	Leadset identification line 2
D3	Leadset input channel 95
D4	Leadset input channel 91
D5	Leadset input channel 88
D6	Leadset input channel 84
D7	Leadset input channel 81
D8	Leadset input channel 77

(Table continued on next page)

Table B-25 (Con't.)
P6480 PIN-TO-MPM/MPX CHANNEL

Pin Number	Description
D9	Leadset input channel 74
D10	Leadset input channel 70
D11	Leadset input channel 67
D12	Leadset input channel 63
D13	Leadset input channel 60
D14	Leadset input channel 56
D15	Leadset input channel 53
D16	Leadset input channel 49
D17	Leadset input channel 14
D18	Leadset input channel 10
D19	Ground
D20	Leadset input channel 4
D21	Leadset input channel 1
D22	Leadset input channel 46
D23	Leadset input channel 42
D24	Leadset input channel 39
D25	Leadset input channel 35
D26	Leadset input channel 32
D27	Leadset input channel 28
D28	Leadset input channel 25
D29	Leadset input channel 21
D30	Leadset input channel 18

Appendix C
Options and Accessories

MPM/MPX OPTIONAL ACCESSORIES

Microprocessor Analysis Modules (MPM/MPX) Standard Application Software Disk (063-0191-00)

Standard Flying Leadset (012-1230-00) with:
Package of 12 grabber tips (020-1386-01)

High Resolution Flying Leadset (012-1231-00) with:
10 ground/signal pair leadsets (196-2963-00)
2 packages of 12 grabber tips (020-1386-01)

General Purpose Probe Adapter (010-6618-00) (for P6480)

Ground/signal pair leadset without series terminator (196-2963-00) (requires 10 per high resolution leadset)

Package of 12 grabber tips (020-1386-01) (requires 20 grabbers per high resolution leadset)

Package of 2 10-wide podlet gang connectors (020-1442-00)

120-pin in-line male DIN connector (131-4443-00) (replaces probe adapter)
120-pin right-angle male DIN connector (131-4039-00) (replaces probe adapter)

671-0071-01/671-0070-01 MPM/MPX Service Manual w/Binder (070-6677-00)

DISK MNEMONICS PRODUCTS

30DM04 8086/8088 Mnemonic Disassembly

Standard Accessories

8086/8088 Mnemonic Disassembly disk and DIP Probe Adapter (socketed) with:
disk (062-9955-00)
8086/8088 DIP Probe Adapter (socketed) (010-6610-00)
30DM04 8086/8088 Mnemonic Disassembly User's Manual (070-7361-00)
4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter
Option 1S Support for 40-pin DIP (Soldered) add:
8086/8088 DIP Probe Adapter (Soldered) (010-6631-00);
delete 8086/8088 DIP Probe Adapter (Socketed) (010-6610-00)

30DM06 80186/80188 Mnemonic Disassembly

Standard Accessories

80186/80188 Mnemonic Disassembly disk and PGA Probe Adapter (socketed) with:
- disk (062-9957-00)
- 80186/80188 PGA Probe Adapter (socketed) (010-6611-00)
- 30DM06 80186/80188 Mnemonic Disassembly User's Manual (070-7362-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter
Option 1S Support for 68-pin PLCC (Socketed) add:
- 80186/80188 PLCC-to-PGA Test Clip (103-0293-00)
- 80186/80188 PGA-to-PLCC Test Clip (103-0292-00)

Option 2S Support for 68-pin LCC (Socketed) add:
- 80186/80188 LCC-to-PGA Test Clip (103-0294-00)

PGA Socket (136-0921-00)
LCC Socket (136-1023-00)

30DM08 80286 Mnemonic Disassembly

Standard Accessories

80286 Mnemonic Disassembly disk and PGA Probe Adapter (socketed) with:
- disk (062-9958-00)
- 80286 PGA Probe Adapter (socketed) (010-6613-00)
- 30DM08 80286 Mnemonic Disassembly User's Manual (070-7364-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter
Option 1S Support for 68-pin PLCC (Socketed) add:
- 80286 PLCC-to-PGA Test Clip (103-0293-00)
- 80286 PGA-to-PLCC Test Clip (103-0292-00)

Option 2S Support for 68-pin LCC (Socketed) add:
- 80286 LCC-to-PGA Test Clip (103-0294-00)

PGA Socket (136-0921-00)
LCC Socket (136-1023-00)

30DM09 80386 Mnemonic Disassembly

Standard Accessories

80386 Mnemonic Disassembly disk and PGA Probe Adapter (socketed) with:
- disk (062-9959-00)
- 80386 PGA Probe Adapter (socketed) (010-0475-00)
- 30DM09 80386 Mnemonic Disassembly User's Manual (070-7365-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter

30DM27 68000/10 Mnemonic Disassembly

Standard Accessories

30DM27 68000/10 Mnemonic Disassembly disk and DIP Probe Adapter (socketed) with:
- disk (062-9960-00)
- 68000/10 DIP Probe Adapter (socketed) (010-6615-00)
- 30DM27 68000/10 Mnemonic Disassembly User's Manual (070-7366-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter
Option 1S Support for 68000/10 DIP (Soldered) add:
- 68000/10 DIP Probe Adapter (Soldered) (010-0487-00);
- delete: 68000/10 DIP Probe Adapter (Socketed) (010-6615-00)

Option 2S Support for 68000/10 68-pin PGA (Socketed) add:
- 68000/10 PGA Probe Adapter (Socketed) (010-6616-00;
- delete 68000/10 DIP Probe Adapter (Socketed) (010-6615-00)

Option 3S Support for 68000/10 68-pin PLCC (Socketed) add:
- 68000/10 PGA Probe Adapter (socketed) (010-6616-00)
- 68000/10 PLCC-to-PGA Test clip 68000/10 (103-0296-00 & 103-0297-00)
- 68000/10 PGA-to-PLCC- test clip ;
- delete 68000/10 DIP Probe Adapter (socketed) (010-6615-00)

Option 4S Support for 68000/10 68-pin PLCC (Soldered) add:
- General Purpose Probe Adapter (010-6618-00)
- 68000/10 PLCC Test Clip
- delete 68000/10 DIP Probe Adapter (socketed) (010-6615-00)

68000/10 PLCC-to-PGA Test clip (013-0250-00)

30DM31 68020 Mnemonic Disassembly

Standard Accessories

30DM31 68020 Mnemonic Disassembly disk and PGA Probe Adapter (socketed) with:
- disk (062-9961-00)
- 68020 PGA Probe Adapter (socketed) (010-6617-00)
- 30DM31 68020 Mnemonic Disassembly User's Manual (070-7369-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter

30DM33 68030 Mnemonic Disassembly

Standard Accessories

30DM33 68030 Mnemonic Disassembly Disk and PGA Probe Adapter (socketed) with:
- disk (062-9962-00)
- 68030 PGA Probe Adapter (socketed) (010-0485-00)
- 30DM33 68030 Mnemonic Disassembly User's Manual (070-7368-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter

30DM41 Z80 Mnemonic Disassembly

Standard Accessories

30DM41 Z80 Mnemonic Disassembly disk and DIP Probe Adapter (socketed) with:
- disk (062-9963-00)
- Z80 DIP Probe Adapter (socketed) (010-6609-00)
- Z80 Mnemonic Disassembly User's Manual (070-7369-00)
- 4 probe latches (105-1007-00)

Optional Accessories

Option 1D Delete the Probe Adapter

Option 1S Support for 40-pin DIP (Soldered) add:
- Z80 DIP Probe Adapter (Soldered) (010-0488-00);
- delete Z80 DIP Probe Adapter (socketed) (010-6609-00)

PERFORMANCE ANALYSIS

30DA01 Performance Analysis Software with:
- disk (063-0192-00)
- PA User's Manual (070-7440-00)

PROTOTYPE DEBUG TOOL PRODUCTS

30RP1 General Purpose Prototype Debug Tool with ROM Probe

Standard Accessories

GP PDT disk (062-9589-00)
GP PDT manual (070-7441-00)
6 foot RP1-to-MPM/MPX cable (174-1461-00)
6 inch RP1-to-RP1 Cable (174-1467-00)
28-pin DIP ROM Probe Adapter (010-6626-00)
32-pin DIP ROM Probe Adapter (010-6627-00)
4 grabber tips (206-0364-00)
4 probe latches (105-1007-00)

Optional Accessories

Option M1 Service
Option M2 Service
Option M3 Service
Option 1M Add Service Manual
include PDT Service Manual Addendum (070-7414-00)
Option 2M Add: Service Maintenance Kit
Option 01 Add: 24/28/32-pin General Purpose ROM Probe Adapter (010-0479-00)
Option 02 Add 40-pin DIP ROM Probe Adapter (010-6628-00)
Option 88 Configured System (can only put 4 30RP1's together)

30DD27 68000/010 Prototype Debug Tool

Standard Accessories

30DD27 68000/010 Prototype Debug Tool Disk with:
disk (062-9596-00)
30DD27 68000/010 Prototype Debug Tool User's Manual (070-7443-00)

30RP1 General Purpose Prototype Debug Tool with ROM Probe

Optional Accessories

24/28/32-pin General Purpose ROM Probe Adaptor (010-0479-00)
28-pin DIP ROM Probe Adaptor (010-6626-00)
32-pin DIP ROM Probe Adaptor (010-6627-00)
40-pin DIP ROM Probe Adaptor (010-6628-00)

96-pin in-line female DIN connector (30RP1 only) (131-2864-00)
96-pin right-angle female DIN connector (30RP1 only) (131-2964-00)
Package of 12 grabber tips (020-1386-01)
PDT Service Manual Addendum (070-7414-00)

FasTrak Products

FasTrak Microprocessor Training Package Standard Accessories

FasTrak Board
110 VAC (119-3680-00)
12 Spare Jumpers (131-0993-00)

FasTrak Microprocessor Training Package Optional Accessories

Option 2P substitute: 220VAC International Power Adapter (119-3681-00)
Option 1W add: PRISM 3000 Microprocessor Workbook

Glossary

Action — In the State Section Trigger Specification, instructions that the analyzer must carry out when a test is satisfied.

Acquisition — The sampling of data from a system under test by a logic analyzer.

Acquisition Clock — The clock that determines the point in time at which the logic analyzer samples data.

Asynchronous Clocking — Clocking that is not related to the SUT's clock.

Asynchronous Clocking Mode — In the State Section, clocking in which sample points are determined by the analyzer at a speed you choose

Channel — An input signal that is assigned a number by which you can identify each signal from the probe.

Channel Group — A defined organization of a number of inputs to form a meaningful combination, such as a 16-bit or 32-bit word.

Clock Line — In the State Section, an input line that is edge-sensitive and can be connected to the SUT clock. A clock line can be combined with other clock and qualifier lines to define when the data sample points occur.

CMOS — Acronym for Complementary Metal Oxide Semiconductor. In the Timing Section, CMOS threshold voltage is ±2.5 V.

Condition — In the State Section Trigger Specification, a user-defined circuit event that the analyzer can recognize.

Counter Condition — In the State Section Trigger Specification, a condition that keeps track of the number of occurrences of defined events.

Demultiplexing Clocking Mode — In the State Section, clocking in which a two-phase sample is taken. You can set up two synchronous clocks to perform two-state clocking to allow you to acquire data from multiplexed lines, or from separate lines with alternating clocks.

DIP — Dual In-Line Package, a microprocessor package style supported by Mnemonic Disassembly in the State Section.

Emulator A piece of development equipment that is used to temporarily substitute read/write memory for read only memory in a system under test.

ECL Acronym for Emitter-Coupled Logic. In the Timing Section, ECL threshold voltage is -1.3 V.

EPROM Erasable Programmable Read Only Memory.

Falling Edge The transition from high to low.

General Action In the State Section Trigger Specification, an optional instruction for the analyzer to perform if the test is met.

General Purpose Probe Adapter A flying leadset with 96 leads, used to make acquisitions in the State Section.

Ground A 0 V condition, usually the reference from which system voltages are measured.

Hold time The amount of time a signal must be valid *after* the clock edge occurs in order to be recognized.

Leadset The hardware that connects the probe to the SUT, usually composed of a connector to the probe, a plastic housing that sometimes contains a circuit board, and cables or leads with connectors that attach to the SUT.

Memory Depth The amount of memory set aside to store a acquisitions.

Memory Partition The proportion of memory set aside for each trigger when using more than one trigger. When more than one trigger is specified, the partition for each trigger will be the same size.

Multiplexed Clocking In the State Section, clocking in which a two-phase clock, allowing samples to be taken at either of two points in time.

P6480 The probe used to make acquisitions in the State Secdtion.

P6486 The probe used to make acquisitions in the Timing Section.

PGA Pin Grid Array, a microprocessor package style supported by Mnemonic Disassembly in the State Section.

PLCC Plastic Leaded Chip Carrier, a microprocessor package style supported by Mnemonic Disassembly in the State Section.

Post-fill memory That part of the acquisition stored after the trigger event.

Pre-fill memory — That part of the acquisition stored before the trigger event.

Probe — The hardware that connects the mainframe to a leadset, usually composed of a connector to the mainframe, a cable, a plastic housing containing a circuit board, and a connector to the leadset.

Probe Adapter — The hardware that connects the probe to the SUT, usually composed of a connector to the probe, a plastic housing containing a circuit board, one or more cables, and a microprocessor socketthat plugs into to the SUT.

Qualifier Line — In the State Section Trigger Specification, an input line that is level-sensitive and can be combined with other clock and qualifier lines to define when the data sample points occur.

Reference — A voltage from which system voltages are measured Usually this is ground, or 0 V.

Rising Edge — The transition from low to high.

Setup time — The amount of time a signal must be valid *before* the clock edge occurs in order to be recognized.

Signal Condition — In the State Section Trigger Specification, a condition that looks for a high or a low signal that was sent from another module or module section.

State — In the State Section Trigger Specification, the combination of the results of one or more tests.

State Control Action — In the State Section Trigger Specification, a mandatory instruction for the analyzer to perform if the test is met.

SUT — System Under Test.

Synchronous Acquisition — An acquisition in which the data sampling occurs each time the SUT clock pulses.

Synchronous Clocking Mode — In the State Section, clocking that is tied to the SUT's clock.

Synchronous Acquisition Mode — In the Timing Section, clocking in which sample points occur with the SUT's clock

Test — In the State Section Trigger Specification, the combination of conditions and subsequent actions.

Timer Condition — In the State Section Trigger Specification, a condition that keeps track of the amount of time between two events.

Transitional acquisition — In the Timing Section, an acquisition in which data sampling occurs each time any channel changes its logic level.

Trigger — In the State Section Trigger Specification, a test that, when met, causes the analyzer to initiate one or more actions.

Trigger Arming — In the Timing Section, a condition that must be satisfied (usually a signal from another module) before the analyzer will begin to test the data.

TTL — Acronym for Transistor-Transistor Logic. In the Timing Section, TTL threshold voltage is 1.4 V.

Word Recognizer Condition — In the State Section Trigger Specification, a condition that defines a word in any of four radixes.

Index

10/10 (high performance leadset) 3-2
10/2 (standardleadset) 3-3

A

acquisition 3-12, 4-23
    synchronous 3-16
acquisition clock definition 2-13
acquisition memory 3-30
acquisition mode 3-14, 4-18
    synchronous 3-16, 3-17 *through* 3-18
    transitional 3-16 *through* 3-17
Acquisition Status screen 3-28, 4-23
acquisition threshold 3-20 *through* 3-21
action 2-23, 3-15, 3-21, 3-27
adapter
    general purpose probe 2-3
    disassembly probe 4-1
application module 1-1
arming 3-15, 3-21, 3-25

B

Boolean Operator field 2-33

C

channel 3-21, 3-23
channel group *see* channel grouping
channel grouping 2-4, 2-6, 2-19 *through* 2-23, 2-28, 3-13, 3-15, 3-21 *through* 3-25, 3-23, 4-17, 4-20
    adding channels 2-22
    assigning to clock phase 2-23
    considerations 2-21
    defining 2-19 *through* 2-23, 4-18
    deleting channels 2-22
    effect of demultiplex mode on 2-18
    in Clocking/Grouping submenu 2-11
    joining channels 2-22
    names 2-20
    splitting channel 2-23
clock 2-17
    acquisition 2-6
    defining acquisition 2-11
clock channels 2-21
clock definition 2-11, 2-14
    example 2-18

clock input
    defining 2-15
clock line 2-3, 2-13
clock row 2-14
clock speed
    changing 2-13
clock type 2-12, 2-14
clock/qualifier line 2-13
clocking mode
    asynchronous 2-11, 2-13
    demultiplexing 2-11, 2-16 *through* 2-19
    multiplexed 2-11
    synchronous 2-11, 2-13 *through* 2-16
clocking rate 2-13
clocking type, *see* clocking mode
CMOS 3-14, 3-20
conditions 2-33, 2-26 *through* 2-33
    adding and deleting 2-34
Control Flow display 4-27

D

data burst 3-16
data sampling rate 3-28
description of PDT, 1-3
description of Performance Analysis, 1-3
description of State Section, 1-2
description of Timing Section, 1-4
disassembler installation 4-2 *through* 4-16
    socketed DIP 4-7 *through* 4-8
    socketed PGA 4-10 *through* 4-12
    socketed PLCC 4-12 *through* 4-14
    software 4-2 *through* 4-4, 4-16
    soldered DIP 4-8 *through* 4-10
    soldered PLCC 4-14 *through* 4-16
disassembly probe adapter 4-1
    connecting *see* disassembler installation
display
    special characters 4-29
DMA cycles 4-19

E

ECL 3-14, 3-20
emulator 5-1 *through* 5-5
EPROM 5-1, *through* 5-5

F

FasTrak 3-4, 3-6, 3-7, 3-9, 4-2
    acquiring data 3-6
    circuit board pin locations 3-6
    connecting mainframe to 3-4
    connection figure 3-4
    steps, acquiring data 3-9
function keys
    manipulating groups 2-20

G

general action 2-33, 2-36
general purpose probe adapter 2-3
GPPA (general purpose probe adapter) 2-3
ground 3-2
group *see* channel group *and* channel grouping

H

Hardware display menu 4-25
high performance leadset 3-2
hold time 2-18, 3-17 *through* 3-18

L

leadset 2-2, 2-8, 3-1
    10/2 (standard leadset) 3-3
    10/10 (high performance) 3-2
    color channel number 3-3
    connecting 2-5, 3-3
    General Purpose Probe Adapter 2-3
    high performance 3-2
    standard 3-2
    minimum setup and hold times 3-18
    special purpose 2-5
load from cursor function 3-15

M

mark cycle function 4-30
memory 2-9, 2-10 *through* 2-11
    acquisition 2-9, 2-40, 3-19
    post-fill 2-10
    pre-fill 2-10
memory depth 2-8, 2-9, 3-16
    choosing 2-7
    definition 2-8
memory partition 2-7, 2-8, 2-9
menu
    timing section setup 3-14

microprocessor (mnemonic) disassembly 1-2
module 1-1

O

occurence number 2-33

P

P6480 (state probe) 2-5, 4-1
    connecting 2-5
    disassembler adapter 4-5
P6486 (timing probe) 3-1
PDT 1-3, 5-1 *through* 5-5
    with other tools 5-5
PDT advantages, 5-5
PDT description, 1-3, 5-1
PDT applications, 5-5
post-trigger 3-19, 3-27
pre-trigger 3-19
probe
    connecting 2-5, 3-1, 3-3, 3-17
    defined 2-2
    disassembler adapter 4-5, 4-6
    ID 3-2, 4-4
    P6480 (state) 2-2, 2-3, 4-4
    P6486 (timing) 3-1
    PDT 5-2, 5-3, 5-4
    relationship to leadset 2-2
    signal latching 2-19
    state 2-2, 2-3, 4-4
    timing 3-1
probe adapter 4-1
probe clock edge 3-14
probe latches 2-5, 4-1
Processor Support submenu 4-29, 4-30

Q

qualifier line 2-13

R

radix 2-28 *through* 2-29, 3-24 *through* 3-26
    changing 2-27, 3-15, 3-26
reference 3-2
reference memory 3-30
resistor color code 3-3
resolution, timestamping 1-2
ROM emulation, 5-1 *through* 5-3

S

set signal 3-27
setup time 2-18, 3-17 *through* 3-18
signal
    identifying 2-32
    intermodule communication with 2-26
    latching 2-19
    related to channel 2-19
    related to state 2-1
signal 2-15, 2-27, 2-28, 2-31, 2-33, 2-37, 3-13
signal conditions 2-27, 2-32
signal in 3-15
signal number 2-32
signal value 2-32
Software display 4-26
split screen 3-15, 4-31
Split Screen display 4-29
standard leadset 3-2
state 2-25, 2-33, 2-35
    defined 2-23, 2-25
    deleting 2-35
    forming from tests 2-23
    multiple tests in 2-35
state analysis 2-7
state control actions 2-33, 2-35, 2-36
State display 4-23
state probe (*see* P6480)
state section
    capabilities 2-1
    choosing 2-6
    connections 2-1
    turning off 2-8
State Section 1-1, 2-5
State Table display 2-5, 4-24
Subroutine display 4-28
symbols 2-29, 3-24 *through* 3-25, 4-21 *through* 4-22

T

test
    conditions *see* conditions
    deleting 2-35
    multiple conditions of 2-34
    related to state 2-24
test 2-23 *through* 2-25, 2-33 *through* 2-35, 3-21, 3-26
test symbol 2-28
threshold voltage 3-13, 3-14
timestamp 3-28 *through* 3-29

Timing Section
capabilities 3-1
choosing 3-14
connections 3-1 *through* 3-2
turning off 3-18
triggers
number of 2-7, 2-9
trigger 2-6, 4-23
trigger conditions *see* conditions
trigger event 3-15, 3-27
trigger location 2-9 *through* 2-11, 3-14, 3-19 *through* 3-20
trigger out 3-27
trigger position 2-9 *through* 2-11, 3-14, 3-19 *through* 3-20
trigger section 3-27
trigger specification 1-2, 2-1, 2-23 *through* 2-26
trigger system 3-27
trigger test 3-15
TTL 3-14, 3-20
two-state clocking 2-11, 2-16

V

VAR 3-20
variable 3-14
voltage
acquisition threshold 3-20

Tektronix®
COMMITTED TO EXCELLENCE

Release Notes

Product Name: 30MPX Microprocessor Analysis Module
Product Line: PRISM 3000 Series Logic Analyzers
Nomenclature: 30MPX or 3001MPX
Version: V1.8

VERSION DIFFERENCES AND ENHANCEMENTS

The following items describe characteristics of the current release of the 30MPX application module software that differ from Version 1.0:

- Compatibility with PRISM System Software Version 2.x
- Special driver required for PDT operation now included in the 30MPX application software (formerly provided separately)
- Software fixes for bugs that were not previously documented

INSTALLATION NOTES

To use this version of MPX software, your PRISM system must be equipped as follows:

- 30MPX board, installed
- PRISM System Software Version 2.0 (or later)

OPERATIONAL NOTES

The following note describes a function associated with this version of software that can affect how you use the PRISM system. The listed function is a high-impact or frequently-seen problem. You should keep these release notes in the Change Information section following the yellow divider page at the rear of the manual.

Changing Word Recognizer Radix

Be careful when changing word recognizer radixes in the Define Condition submenu (accessed from the MPX State Section menu). If you have more than one word recognizer defined, do not change a radix in the first word recognizer. Doing so can cause an irrecoverable error, requiring that you cycle power to the system. Changing a radix in the second (or later) word recognizer does not cause any problems.

061-3874-00
Product Group 5E

First Printing: JUL 1991

UPDATE ON SOFTWARE FUNCTIONS

The following note describes a function associated with this release of the PRISM System Software. The listed function is a high-impact or frequently-seen problem.

Rising and Falling Edge Transitions in the Vertical Display

Changing the Time/Div setting when you have Vertical Display enabled may invalidate the accuracy of the Vertical Display value. If you change the Time/Div setting, you should also reposition the cursor for an accurate reading.